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Research and Development Technical Report

ECOM-72-0005-F

DETERMINATION OF THE BEST SET OF CHARACTERISTICS FOR AN U.S. ARMY DIGITAL CARD TESTER

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A study to determine the best set of characteristics for a semi-automatic, general purpose digital card tester (DCT); to estimate its cost; and to describe its intended applications. The study, ~~which~~ culminated in the development of a recommended set of characteristics for an Army DCT based on US Army maintenance concepts, fault detection/isolation requirements, and related cost data, complements the efforts of the US Army Electronics Command Test, Measurement, and Diagnostic Equipment (TMDE) Standardization Program.

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FOREWORD

Under a 180-day contract starting 12 May 1977, ARINC Research Corporation provided non-personal services to the U.S. Army Electronics Command (ECOM) to determine the best set of characteristics for a digital card tester (DCT). The contract was issued by the Procurement Division, Headquarters, Fort Huachuca, as modification number 8 under Contract DAEA 18-72-A-0005, delivery order 0007, a basic ordering agreement. This report presents the results of the contract effort.

ARINC Research Corporation wishes to acknowledge the invaluable assistance of Mr. Frank Mihlon and Mr. Robert Both of the U.S. Army Electronics Command, Directorate of Maintenance, TMDE Division. We also wish to thank Mr. James Carter, Chief TMDE Division, for his interest and guidance during the study.

Finally, we wish to express our thanks to the other U.S. Army Commands and individuals and DCT manufacturers who have assisted this study through their advice, submission of materials, and responsiveness to the DCT survey forms.

SUMMARY

ARINC Research Corporation, in support of the U.S. Army Electronics Command (ECOM) Test, Measurement, and Diagnostic Equipment (TMDE) Standardization Program, conducted a study to determine the best set of characteristics for a digital card tester (DCT). The period of performance of this project was six months, beginning 12 May 1977.

The overall objective of this study was to determine the best set of characteristics for a semi-automatic, general purpose DCT; to estimate DCT hardware and software costs, and to describe the intended DCT applications. To accomplish these objectives, the program was subdivided into seven major tasks. The results of Tasks 1 through 6 are contained in the body of this report. The results of Task 7, which entails the development of DCT parameters, are contained in Appendix H.

The basis of the study consisted of technical data obtained from a variety of publications and information requested by means of two separate survey forms. One form, "DCT Capabilities Survey" was directed at 11 DCT manufacturers for 13 specific DCT model numbers. The second form, "DCT Maintenance Application Concepts Survey", was sent to 90 current and potential users of DCTs in the U.S. Army. The data received were analyzed within the constraints listed in Table S-1. These constraints were established by joint decision of ECOM and ARINC Research Corporation in order to focus the survey responses of the DCT manufacturers on U.S. Army requirements.

The survey results indicated that there are several models of DCTs that are within the constraints, some of which have already been procured by DoD activities, including the Army.

The Army survey participants recognized the need for an Army Standard DCT and, if it existed, would consider its applicability to the support of their respective electronic systems. However, the requirements for the DCT have not been quantified to the point where immediate procurement activities are practical.

Table S-1. DCT STUDY CONSTRAINTS
• The DCT must be procurable off the shelf (OTS).
• The DCT must be portable and capable of operating from either 50/60 or 400 Hz 115/230 Vac power sources. (The DCT can be modified to meet this constraint.)
• The DCT must not exceed three separate units, exclusive of program files, accessories, and external test equipment.
• The total weight of the DCT must not exceed 200 pounds (90.72 kilograms), with no individual unit exceeding 95 pounds (43.1 kilograms).
• The cost of each DCT system -- less Test Program Set (TPS) cost -- must not exceed $50,000.
• The DCT must be programmable in the field by a skilled electronics repair technician.

The surveyed DCTs were categorized into three groups on the basis of their respective test methods and program generating source. Group 1 consists of self-contained DCTs, i.e., DCTs that can develop programs and test Printed Circuit Boards (PCBs). Group 2 consists of "test only" units, and Group 3 consists of DCTs that use the "smart probe" test method. From the analysis that followed, it was concluded that the Group 1 units best met the DCT maintenance application requirements of the Army. These units are characterized by their self-programming ability and their test method, which is defined as an edge connector with a guided probe. The best set of characteristics for a semi-automatic general purpose digital card tester (presented in Appendix H) is derived from the Group 1 characteristics.

The DCT hardware/software cost, less the cost of Test Program Sets (TPSs), ranges from $7870 to $70,925 and is dependent on test capabilities, test methods, and displays of the individual DCT. The Group 1 testers are priced under $20,000 per unit.

A TPS consists of documentation and a program (contained on a storage device) that is applicable to a specific model of Printed Circuit Board (PCB) and an interface device/adapter that is normally usable with more than one model of PCB. TPSs are not interchangeable between different DCT manufacturers' model numbers. TPS costs involve acquisition and possible TPS modification and duplication. On the basis of cost estimates to develop TPSs for five PCBs, as provided by DCT manufacturers who participated in the DCT capabilities survey, TPS cost ranges from a low of $96 to a high of $5800 per TPS. The average cost is $1474 for a TPS with maximum fault-detection/isolation test capability and $1183 for a "go/no-go" test capability.

The DCT's maintenance application must complement the current and future maintenance concepts of the Army and fill an existing and anticipated void in this structure. For the DCT to become a part of this framework, its primary maintenance role should be in go/no-go PCB testing. A secondary function of "component isolation" for low-density electronic systems should also be considered for the DCT. However, this function should be considered only in conjunction with the Army's planned Automatic Test Equipment (ATE) Automatic Test Support System (ATSS), for which the major role of component isolation has been reserved in the future.

While not in total harmony with envisioned U.S. Army requirements, as depicted by the U.S. Army survey participants, the surveyed DCT manufacturers' equipment capabilities are compatible with these requirements.

It is recommended that ECOM proceed with the preparation of a DCT specification while continuing to qualify and quantify the requirements for an Army Standard DCT. It is further recommended that as a part of the Army DCT program, a "DCT Applications Planning Guide" be developed. This guide, which would assist program managers in determining the applicability of a DCT to their system support requirements, should include a detailed TPS specification for subsequent TPS development.

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CHAPTER ONE

INTRODUCTION

1.1 BACKGROUND

Over the past several years, the U.S. Army has been purchasing and deploying increasing numbers of electronic systems designed and manufactured to the latest digital electronic switching technology. This trend is expected to continue into the foreseeable future. These electronic systems include printed circuit boards (PCBs), in a variety of sizes, shapes, and layouts, that use various types of integrated circuits (ICs) as their primary components. The PCBs may contain from 1 to more than 100 ICs, which may constitute a pure digital PCB or combine with analog components to form a hybrid PCB.

The application of digital technology has drastically altered field maintenance concepts and procedures for electronic systems, essentially reducing equipment maintenance in the field to fault isolation, removal, and replacement of PCBs. The defective units are then sent for repair to a higher level of maintenance. This procedure has increased the maintenance responsibilities and requirements for associated skills and support equipments at the field intermediate maintenance points -- i.e., Direct Support and General Support, where the PCBs are received, repaired, and stored. Because of the numerous configurations and electrical parameters of the PCBs, a large complement of general and special purpose Test, Measurement, and Diagnostic Equipment (TMDE) is required to fault-detect/isolate to the defective IC. In addition, to verify the operational condition of the PCB, a "hot mock-up", consisting of the major segments of the end item, is required. Further, the fault-detection/isolation and repair process is complicated and time-consuming and constitutes a drain on critical equipment and manpower resources.

In 1976, it became apparent that some kind of general purpose maintenance aid was required to assist in quickly determining the go/no-go condition of PCBs, using digital technology, and fault-isolating to the defective IC. Further, the increasing numbers of digital PCBs entering the Army-wide inventory make it necessary to reduce significantly the individual diagnostic time for each board. Commercial firms are addressing this problem by using semi-automatic general or special purpose Digital Card Testers (DCTs) to meet their requirements. This approach represents a potential solution to the Army's digital PCB test problems. However, the selection and application of DCTs must complement the existing and anticipated changes to the U.S. Army maintenance concepts if the DCT is to become a useful element in the TMDE planning structure.

ECOM has recognized the digital PCB test problem and its impact on material readiness and existing maintenance concepts, as well as the consequent need to standardize TMDE throughout the U.S. Army. To address these requirements, in May 1977 ECOM awarded a contract to ARINC Research Corporation to determine the best set of characteristics for a DCT, estimate the hardware and software cost, and describe intended DCT applications within the Army maintenance structure.

1.2 STUDY OBJECTIVES

The overall objective of the program was to determine the characteristics of a DCT that would best suit U.S. Army requirements to test digital PCBs. Specific study objectives were as follows:

- Determine the best set of characteristics for a semi-automatic general purpose DCT
- Estimate the basic hardware/software cost of a DCT
- Determine the best maintenance support application(s) for an Army-adopted DCT

1.3 OVERVIEW OF WORK PERFORMED

Achievement of the program objectives involved a series of interrelated tasks as diagrammed in Figure 1-1:

1. Evaluate the Semi-Automatic General Purpose DCT Market
2. Develop and Distribute a DCT Capabilities Survey Form
3. Develop and Distribute a DCT Applications Survey Form
4. Review and Summarize DCT Characteristics
5. Develop DCT Application Concepts
6. Prepare Final Report
7. Prepare DCT Parameters

In Task 1 various documents and periodicals were reviewed to determine the number of DCT manufacturers that might be included in the study and the technological trends of the DCT industry. This task led to the selection of 13 DCTs manufactured by 11 different companies. The selected DCTs were used as the basis for the capabilities survey of Task 2 and capabilities analysis of Task 4.

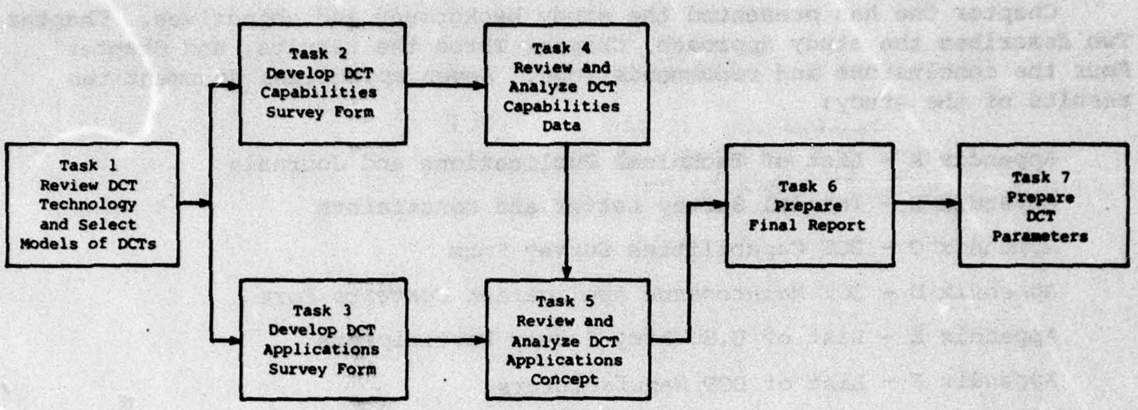

Figure 1-1. OVERALL TECHNICAL APPROACH

In Task 2 a survey form was developed and distributed to the manufacturers selected in Task 1. This form encompassed all the known and anticipated salient features applicable to DCTs. It also included a request to review five digital PCB schematics (and associated documents) and to estimate the cost to develop a Test Program Set (TPS) for each one.

In Task 3 a survey form was developed to assist ECOM in determining the intended applications of DCT within the Army. This survey form, requesting applications data, was sent to 90 different U.S. Army commands, Program Managers, and individuals.

During Task 4 the information received from the capabilities survey of Task 2 was reviewed, cataloged, and displayed in a way that facilitated an overall analysis of the DCTs' respective characteristics, costs, and potential applications.

In Task 5 the information obtained from the surveys in Tasks 3 and 4 was correlated, and a maintenance application concept described that best reflected the requirements of the using commands within the limitations of the DCT. This task resulted in the formulation of maintenance application concepts for DCTs.

In Task 6 this final report was prepared to present the results of each of the previous tasks and the conclusions and recommendations of the program.

In Task 7 the DCT parameters for an Army Standard DCT were identified to facilitate the preparation of a DCT specification by the Army. These parameters reflect the conclusions of ARINC Research Corporation based on the results of Tasks 1 through 6.

1.4 REPORT ORGANIZATION

Chapter One has presented the study background and objectives. Chapter Two describes the study approach, Chapter Three the results, and Chapter Four the conclusions and recommendations. Seven appendixes document the results of the study:

Appendix A - List of Technical Publications and Journals

Appendix B - Initial Survey Letter and Constraints

Appendix C - DCT Capabilities Survey Form

Appendix D - DCT Maintenance Application Concepts Form

Appendix E - List of U.S. Army Survey Participants

Appendix F - List of DCT Manufacturers

Appendix G - TPS Cost, Confidence, and Run-Time Data

Appendix H - Best Set of Characteristics for a Semi-Automatic General Purpose Digital Card Tester (DCT)

CHAPTER TWO

TASK DESCRIPTIONS

2.1 TASK 1: EVALUATE THE SEMI-AUTOMATIC GENERAL PURPOSE DIGITAL CARD TESTER MARKET

A number of documents and periodicals were reviewed to determine the general characteristics and test methodologies of DCTs, the method used to test and service digital PCBs, the technological trends in the DCT industry, and the number of DCT manufacturers that might be included in a DCT study. The significant technical journals and publications reviewed are listed in Appendix A.

From the January 1977 issue of *Circuits Manufacturing*, 64 commercial manufacturers of PCB testers were identified. Each of these potential sources of information on DCTs was sent a letter outlining the U.S. Army DCT program and requesting information. Each letter also contained a list of "constraints", which were formulated to reflect characteristics desired in an Army DCT in order to focus the requested information on U.S. Army requirements. The constraints were subsequently revised as shown in Table S-1 of the Summary of this report. A sample copy of the letter is presented in Appendix B.

The last step in this task, in conjunction with ECOM, was the selection of up to 20 DCTs, by manufacturer's name and model number, that were within or only slightly outside the constraints.

2.2 TASK 2: DEVELOP AND DISTRIBUTE A DCT CAPABILITIES SURVEY FORM

During Task 2 a DCT Capabilities Survey Form was developed and distributed to the DCT manufacturers selected in Task 1. The purpose of this form was to obtain the broad spectrum of information required to determine the best set of characteristics for a DCT, to obtain hardware/software cost data, and to compare DCT capabilities with U.S. Army requirements. The survey form included information on the U.S. Army DCT program, the DCT constraints, and questions related to the characteristics and cost of a particular make or model of DCT. The questions were arranged in eight categories:

- Equipment Description
- General
- Cost
- Operational Capabilities
- Physical
- Support
- Test Program Sets (TPSs)
- Training

In addition, the survey form contained five appendixes. Each appendix was related to a specific PCB found in the U.S. Army inventory and included as a minimum a description of the "theory of operation", a schematic, parts lists, and an illustrated parts breakdown. The DCT manufacturers were asked to estimate the development cost of a TPS for the five PCBs applicable to a specific DCT selected in Task 1.

A copy of the DCT Capabilities Survey Form is presented in Appendix C.

2.3 TASK 3: DEVELOP AND DISTRIBUTE A DCT APPLICATIONS SURVEY FORM

In Task 3 a DCT Maintenance Applications Concept Survey form was developed for distribution within the Army. A copy of this form is presented in Appendix D. The purpose of this survey was to obtain information on DCT maintenance application concepts, material requirements, and training in order to provide ECOM with a comprehensive understanding of the scope of the Army's requirements for a DCT. The survey was sent to the 90 U.S. Army activities listed in Appendix E. It was divided into three parts to facilitate questions and answers. Part I contained general questions; Part II contained questions applicable to current DCT users; and Part III requested information from organizations that expected to employ a DCT within the next five years. In addition, the form provided information on the ECOM DCT program and listed the DCT constraints and the makes and models of DCTs that were selected in Task 1.

2.4 TASK 4: REVIEW AND ANALYZE DCT CHARACTERISTICS

During Task 4 the data received from the various DCT manufacturers requested in Task 2 were reviewed, cataloged, and displayed in such a manner as to facilitate an overall analysis of their respective characteristics, cost, and potential application.

The results of this portion of the study illustrated each major characteristic and permitted a comparison among various DCT models. These data were used to develop the best set of characteristics for a semi-automatic general purpose digital card tester; they also provided the basis for the identification of DCT parameters in Task 7.

2.5 TASK 5: DEVELOP DCT APPLICATIONS CONCEPT

In Task 5 the information obtained in Tasks 3 and 4 was correlated, and a maintenance applications concept was described that best meets the requirements of the using commands within the limitations of the DCT. The survey data were also analyzed to determine whether the application of a DCT device will affect the requirements for general purpose OTS TMDE and existing ATE.

2.6 TASK 6: PREPARE FINAL REPORT

This final report was prepared to present the results of each task and the conclusions and recommendations of the study.

2.7 TASK 7: PREPARE PARAMETERS FOR DCT

Task 7 resulted in the identification DCT parameters for subsequent formulation by the Army into a DCT specification that conforms with MIL-T-28800 Type III, Class 5, Style E, Color R. This identification was based on the data obtained in Tasks 1 through 5.

CHAPTER THREE

STUDY RESULTS

3.1 EVALUATION OF THE SEMI-AUTOMATIC GENERAL PURPOSE DCT MARKET

3.1.1 Selection of Up to 20 Digital Card Testers

From the responses to the initial survey letter mailed to the 64 manufacturers of DCT devices, 7 DCTs were selected as DCT survey candidates. Six additional DCT candidates were selected on the basis of recommendations from U.S. Army activities and DCT manufacturers and a review of advertisements in periodicals. The 13 DCT candidates are listed in Table 3-1. The full name and address of each company is listed in Appendix F.

Table 3-1. DCT SURVEY CANDIDATES

Manufacturer	Model
Bendix	13A9070
Data Tester	5800
Digital General	ELF
Fluke	1000A 3010A
General Dynamics	ICT-105
GenRad	GR-DCT
Hughes	HC-192
Mirco System	520
Systron Donner	3700P
Technoloogy Marketing	2160
Testline	2200 2300

3.1.2 Technology Trends

As a result of the review of technical journals and publications, technological trends related to DCTs were divided into two interrelated areas, Printed Circuit Boards (PCBs) and Digital Card Testers (DCTs). These trends are discussed below.

3.1.2.1 Printed Circuit Boards (PCBs)

The complexity of digital PCBs will continue to increase as technological advancements and improvements expand the number of functions per chip (higher integration). Further, the number of applications amenable to digital technology is increasing. With each new advance in integrated circuit (IC) technology, the testing of these circuits becomes significantly more difficult. The testability of a digital PCB can be expressed by the following qualitative relationship:

$$\text{Testability} = \frac{\text{Number of Access Points}}{\text{Number of Functions per Chip}} + \text{Design for Testability}$$

Since the number of access points is usually limited by the number of pins of the edge connector, an increase in the number of functions per chip decreases the testability of the PCB. Designing a PCB to be testable on a particular DCT (Design for Testability) adds a second factor, which increases the testability of the PCB. However, the application of the Design for Testability concept to PCBs, while significant, will have a diminishing impact as the number of functions per chip continues to increase.

Because of this increasing number of functions per chip versus access points and the need to verify digital PCB reliability at the production point, it is expected that the trends in the DCT industry will be toward smaller dedicated testers at the expense of larger, flexible, general purpose systems. These testers will be concerned primarily with verifying the manufacturing process of PCBs -- i.e., solving production problems rather than field problems, which are concerned with restoring a PCB to operational status. This emphasis is understandable inasmuch as the major segment of the DCT market is associated with production-line verification of a few types of PCBs in large volume, and the manufacturer's requirement is for a DCT that will perform in his particular application at minimum cost. On the other hand, the field requirements are for a DCT that can fault-detect/isolate multiple types of PCBs in small quantities -- usually no more than one at a time.

3.1.2.2 Digital Card Testers (DCTs)

The DCT industry, like manufacturers of other electronic test systems, is taking advantage of technological improvements in solid-state devices (particularly the microprocessor), circuit design improvements and layouts, and displays and controls. Further, improvements in the man-machine interface of DCTs have reduced the number of operating controls, which has simplified training and operating requirements. These trends have resulted in DCTs with improved accuracy, application, and reliability.

As the trends in semiconductor technology continue toward higher levels of integration, testing of lower levels of integration can be facilitated by applying this higher-level technology to DCTs, increasing their test capability. However, the application of this new technology tends to solve old test problems; i.e., the higher-level integrated devices can test the lower-level integrated devices. It does not allow the DCT to test the higher technology inherent in itself or in some of the newer electronic systems. The microprocessor is a good illustration of the problem: while this device is finding increasing use in DCT design, present DCT technology cannot test it. This is a disadvantage for DCTs; but it is probably not a major disadvantage because of the small population of microprocessors and the ability to verify their operation by other means, such as direct substitution.

Since DCTs are support equipment, they will not push the state of the art but instead will be pulled by it. Therefore, DCTs can be expected to lag behind new technology to varying degrees. This lag could be offset as more manufacturers of electronic systems apply digital technology to their respective product lines and thereby broaden the market.

3.2 REVIEW AND ANALYSIS OF DCT CHARACTERISTICS

The overall response by DCT manufacturers to the DCT Capabilities Survey Form is shown in Table 3-2. GenRad and Technology Marketing did not respond. The Systron-Donner response was received too late to be included in this report.

Table 3-2. RESPONSE TO DCT CAPABILITIES SURVEY FORM

Survey Category	Number
Different DCTs surveyed	13
DCT manufacturers represented	11
DCT manufacturers responding	9
DCTs represented	11

The results of the DCT Capabilities Survey Form are described and illustrated in the following series of discussions, matrices, and tables. Whenever applicable, the source paragraphs from the survey form or other documents are noted. (Data from Systron-Donner are not included in any of the discussions, matrices, or tables.)

3.2.1 DCT Characteristics

Table 3-3 gives the DCT model history for each DCT described in response to the survey. The table includes the date the DCT was first offered on the commercial market, previous models of DCTs from which the surveyed model evolved, and the model number(s) or the DCT family of which the surveyed model is a part.

Table 3-3. DCT MODEL HISTORY (Source: Para. 1.0, Capabilities Survey)

Manufacturer	Model Number	Date First Offered on Commercial Market	Previous Model(s) Offered	DCT Family or Model Number
Bendix	13A9070	Mar 1977	BDX-1	CAFIG (see Bendix Survey Form)
Data Tester	5800	Jan 1977	4800, 4000, 2000	5810 and 5820 tester only; 5855 portable field version of 5800
Digital General	ELF	Oct 1973	Continually improved since introduction	TROLL
Fluke	1000A	Sep 1972	Not identified	Tendar 1010A and 2000A
	3010A	Jun 1975	Not identified	Tendar 3020A
General Dynamics	IC-105	May 1973	ICT-100, 101, 102, 103, and 104	N/A
Hughes	HC-192	Jul 1975	Not identified	N/A
Mirco Systems	520	Jul 1974	525	Series 500
Testline	2200	Jan 1976	Not identified	3000 console, 1000 portable
	2300	Jun 1976	Not identified	3000 console, 1000 portable

Table 3-4 shows the extent of DoD documentation currently available for each DCT and indicates if a specific model of DCT has been procured by a DoD activity within the last year. The numbers procured and the DoD activities involved are listed in the applicable model number's DCT Capabilities Survey form. A review of the various DCTs' operation and maintenance manuals indicated that it would be necessary to develop supporting publications for an Army Standard DCT.

Table 3-4. DCT DoD DOCUMENTATION (Source: Para. 2.0, Capabilities Survey)

Manufacturer	Model Number	Nomenclature	National Stock Number	Technical Publication Number	GSA Schedule Number	Purchased by DoD within Last Year
Bendix	13A9070	None	None	None	None	Yes
Data Tester	5800	None	None	None	GS-00S-04629	No
Digital General	ELF	None	None	None	None	No
Fluke	1000A	None	None	USAF TO33D7-76-70-1 TO33D7-76-70-1	GS-00S-04736	No
	3010A	None	6625-xx-006-5960	None	GS-00S-04736	Yes
General Dynamics	ICT-105	AN/USM-401	6625-00-140-2335	NAVSHIPS 0969-292-0010	GS-00S-04984	Yes
Hughes	HC-192	AN/UYM-7	6625-01-016-1866	USAF T.O. 33AA39-10-1	None	Yes
Mirco Systems	520	None	None	None	GS-00-05022	No
Testline	2200	None	6625-01-034-3772TA	None	GS-00S-05106	No
	2300	None	6625-01-034-3772TA	None	GS-00S-05106	No

DCT hardware Cost Data are presented in Table 3-5. The "Expanded System Cost" includes the unit cost plus the cost of options or other devices that expand the basic DCT model to its maximum test capability. The add-on options, etc., are shown under the "Cost Elements in Expanded System" column.

As a general rule, none of the DCTs surveyed will require supporting TMDE to fault-detect/isolate a PCB. However, with additional supporting TMDE -- e.g., an oscilloscope, function generator, and power supply -- the test capabilities of the DCT can be significantly extended. Further, an oscilloscope can simplify the programming process by displaying the input and output pattern responses. A DCT that can interface and interact with standard general purpose TMDE offers increased testing capability and versatility.

Several DCT manufacturers indicated some capability to perform end-to-end tests on a Line Replaceable Unit (LRU) and to perform a go/no-go test on an analog PCB. The ability to fault-detect to a PCB within an LRU, while perhaps feasible, is not practical, primarily because of the interface device problems associated with each LRU and the design constraints of existing LRUs. However, an LRU designed to be tested by a specific DCT should not present these problems. Only one manufacturer, General Dynamics, emphasized the capability of its instrument (in this case, the ICT-105) to perform a go/no-go test on analog PCBs.

The physical and power characteristics of the surveyed DCTs are listed in Table 3-6. The weight and power requirements noted in the constraints are met by the majority of the DCTs. The exception is the weight of the Data Tester 5800; however, the "test only" version of this model should meet the contraints. All of the DCTs surveyed are of modular solid-state construction.

Environmental characteristics are listed in Table 3-7. The MIL-T-28800B requirements for a Class 5 instrument are depicted across the bottom of the table. A comparison shows that none of the surveyed DCTs meets the MIL-T-28800B requirements completely.

Mean-time-between-failures (MTBF) and mean time-to-repair (MTTR) data for the surveyed DCTs are reflected in Table 3-8. Several of the manufacturers were not familiar with MIL-HDBK-217B and therefore could not fully respond. For the same reason, the MTBF data are of questionable accuracy and should be considered of limited value until subjected to further qualification.

All of the DCTs in the survey have the capability to perform a self-test to indicate that the unit is functioning. Most units also have the capability to fault-isolate to a faulty PCB with varying degrees of accuracy and then to fault-isolate the failed component on the at-fault PCB. (It is assumed that spare modules are available to restore the DCT to an operational status.) The DCT manufacturers provide warranties for their equipment, generally 90 days for parts and labor and one year for parts. Factory repair services are available.

Table 3-5. DCT HARDWARE COST DATA (Source: Para. 1.1.1 and Para. 3.0, Capabilities Survey)

Manufacturer	Model Number	Unit Cost (Dollars)	Expanded-System Cost (Dollars)	Cost Elements in Expanded System	Cost Data Source
Bendix	13A9070	11,500	24,000	Debug, 256 pins, fault isolation, PROM programming, MAG tape	Bendix Survey Form
Data Tester	5800	39,950	52,300	16 pins × 8 boards, 1 multi-level drive, CRT, second floppy disk	GS-00S-04629
Digital General	ELF	7,400	18,480	Options 102,3,4,5,8, and 9; 202 and 4; 316; 530; and 602	Digital General price list dated 1 February 1977
Fluke	1000A	7,475	7,870	200 probe	GS-00S-04736
	3010A	12,900	15,120	200 probe, 3010-900, 3010-592, and 1010-347	GS-00S-04736
General Dynamics	ICT-105	11,933	16,133	AS-101	GS-00S-04984
Hughes	HC-192	13,995	15,390	HC-192/A-1 Programming Panel	Hughes price list dated 15 April 1977
Mirco Systems	520	16,005	29,148	Options 3 (5 each) and 10 (2 each) and the 550 basic unit with 1 each PS502 and PS503	GS-00S-05022
Testline	2200	12,500	20,395	32-pin pulsed power supply and 16-pin slave	GS-00S-05106
	2300	14,500	21,695	32-pin pulsed power supply and 16-pin slave	GS-00S-05106

Table 3-6. DCT PHYSICAL AND POWER CHARACTERISTICS (Source: Para. 5.1 and 5.2, Capabilities Survey)

Manufacturer	Model Number	Weight in Pounds (lb) and Kilograms (kg)	Weight, Height, Depth in Inches (in) and Centimeter (cm)	Power Requirements	Power Consumption in Watts	Remarks
Bendix	13A9070	30 lb 13.6 kg	19 × 8.5 × 18 in 48.2 × 21.5 × 45.8 cm	115/230 Vac, 50-400 Hz	150	
Data Tester	5800	525 lb 238.6 kg	71 × 42 × 39 in 181 × 106.7 × 99.1 cm	115/230 Vac ±10%, 50-60 Hz	900	Power consumption depends on UUT and power supply options.
Digital General	ELF	55 lb 25 kg	20.3 × 9.5 × 22.3 in 51.5 × 24 × 56.5 cm	115/230 Vac , 50/60 Hz	300	AC volts must be specified.
Fluke	1000A	79.4 lb 36 kg	24 × 11.4 × 8.4 in 61 × 29 × 21.4 cm	115/230 Vac, 50-400 Hz	200	Modification required for 400 Hz operations.
	3010A	55 lb 25 kg	22 × 14 × 25 in 55.9 × 35.6 × 63.5 cm	115/230 Vac, 47-440 Hz	300	Requires options 3010-900 for 400 Hz operations.
General Dynamics	ICT-105	75 lb 34 kg	19.7 × 10 × 20.5 in 50 × 26 × 52 cm	115/230 Vac, 50-400, Hz	350	
Hughes	HC-192	86 lb 39 kg	20.5 × 13.8 × 24 in 52 × 35 × 61 cm	115/230 Vac, 50-400 Hz	300	Style E Enclosure (Equipment Case).
Mirco Systems	520	54.7 lb 24.8 kg	23 × 9 × 16 in 58.4 × 22.9 × 40.6 cm	115/230 Vac, 50-400 Hz	270	
Testline	2200	63.15 lb 28.64 kg	21 × 16 × 21.5 in 53.34 × 40.64 × 54.61 cm	125/230 Vac, 50-60 Hz	250	
	2300	76.18 lb 34.55 kg	21 × 16 × 21.5 in 53.34 × 40.64 × 54.61 cm	115/230 Vac, 50-60 Hz	250	

Table 3-7. ENVIRONMENTAL CHARACTERISTICS (Source: Para. 5.5, Capability Survey)

Manufacturer	Model Number	Temperature Range (°C)		Relative Humidity (Percent)	Altitude in Meters (in) and Feet (ft)		Vibration Limits	Fungus Resistance
		Operating	Nonoperating		Operating	Nonoperating		
Bendix	13A9070	0 to 50	-40 to 71	95	3,050 in 10,000 ft	3,050 in 10,000 ft	1.5g	Can be provided
Data Tester	5800	0 to 45	-20 to 65	70	Not specified	Not specified	Not specified	Not specified
Digital General	ELF	10 to 32	-23 to 54	90	3,050 in 10,000 ft	12,000 in 40,000 ft	Not specified	Optional
Fluke	1000A	0 to 50	-20 to 60	95	3,692 in 12,113 ft	15,384 in 50,475 ft	Not specified	Not specified
	3010A	0 to 50	-20 to 60	95	3,692 in 12,113 ft	15,384 in 50,475 ft	Not specified	Not specified
General Dynamics	ICT-105	0 to 50	Not specified	Not specified	3,050 in 10,000 ft	15,240 in 50,000 ft	Not specified	Not specified
Hughes	HC-192	0 to 50	-20 to 60	0 to 95	3,692 in 12,113 ft	15,384 in 50,475 ft	Not evaluated	None
Mirco Systems	520	10 to 49	-55 to 60	10 to 90	3,658 in 12,000 ft	15,240 in 50,000 ft	High	Not specified
Testline	2200	10 to 45	0 to 55	0 to 90	6,100 in 20,000 ft	11,887 in 39,000 ft	Not specified	Not specified
	2300	10 to 45	0 to 55	0 to 90	6,100 in 20,000 ft	11,887 in 39,000 ft	Not specified	Not specified
MIL-T-28800B	Class 5	0 to 50	-55 to 75	95	3,050 in 10,000 ft	12,000 in 40,000 ft	2g maximum	As specified

Table 3-8. DCT MTBF/MTTR DATA (Source: Para. 6.0, Capabilities Survey)					
Manufacturer	Model Number	MTBF (Hours)		MTTR (Minutes)	
		History	Prediction	Restoral	Repair
Bendix	13A9070		3500	10	60
Data Tester	5800		5000		20
Digital General	ELF	2000		15	60
Fluke	1000A		5000	30	
	3010A		3962	22	
General Dynamics	ICT-105		700	18	29
Hughes	HC-192		3962	22	20
Mirco Systems	520	5000		15	15
Testline	2200		4020	30	60
	2300		4020	30	60

The majority of the DCT manufacturers reported that calibration of their instrument was not required. However, a review of their technical documents indicated that adjustments are made periodically to power supplies that provide power to the PCBs being tested. It appears that a good-quality digital multimeter can verify the voltage levels as part of the preventive maintenance routines for the DCT; therefore, calibration of DCTs is not considered a major support problem.

3.2.2 Fault-Detection/Isolation Techniques

The determination of a particular fault-detection/isolation technique for an Army DCT must consider the test capability, the test method, and the logistics required to support the DCT in various roles.

A DCT with test capabilities to test a variety of PCBs dynamically -- i.e., a test that mirrors the test patterns, voltages, rates, etc., that the PCB would encounter in the actual electronic system -- would be the most desirable type of DCT. However, dynamic testing is not within the test capability of any of the DCTs surveyed, nor should this level of test capability be expected within the DCT "constraints" established in Task 1. Dynamic testing is reserved for major computer-controlled test systems, leaving static testing of PCBs for DCTs conforming to the constraints.

A static test is any test that stimulates the PCB or the components on the PCB at a rate or under conditions that are lower than those of the real-time operating environment. All DCTs surveyed are classified as static testers because of their inability to duplicate the actual operating characteristics.

The quality of a static tester can be measured by how closely it can approach a dynamic test for each PCB. Figure 3-1 displays a static test scale of from 1 to 10, with 10 being a dynamic test.

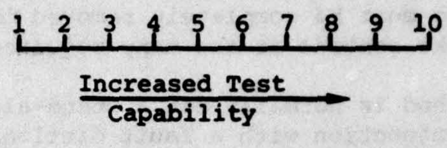

Figure 3-1. STATIC TESTING

Thus the DCT that can test the greatest number of PCBs with a mean test result that is farthest to the right on the static test scale would be the most desirable DCT, assuming all other characteristics are in proportion. However, it is not a simple process to determine the quality of an individual DCT or group DCTs since they have unique characteristics, as do individual PCBs. In order to make such a determination, a number of representative PCBs must be selected in sufficient quantity to provide a predetermined confidence level in the final test results. Next, each of the selected PCBs must be analyzed and tested against each DCT being considered, and the quality of the static test capability must be determined. This can be a time-consuming and costly process, but one that should be considered as part of the procurement process for an Army Standard DCT.

There are several test methods available to test PCBs; they can be broadly categorized as in-circuit, guided probe, "smart probe", and edge connector. Several of the DCTs surveyed use two or more of these methods.

Most of the Army's PCBs are conformally coated, and this will influence the choice of test method and subsequently establish the type of DCT that has application in the Army. Conformal coating is a transparent electrical insulating compound used to protect the PCB from an unfavorable environment. The compounds themselves are made up of a number of types of materials and applied to the PCBs in various degrees of thickness, depending on the mission requirements of the electronic system. As an insulator, conformal coating prevents electrical contact and thus limits the test methods that can readily be used to test a PCB. For example, the coating must be removed for three of the four methods listed above --, in-circuit, guided probe, and smart probe -- in order to test the PCB. Once the PCB is tested and repaired, of course, the coating must be replaced. The logistics effort required to support such an operation is significant.

The planned method for removing and replacing the conformal coating in the Army is centered on the Pace Kit, a sophisticated soldering device that is supplemented with small amounts of conformal coating compounds for use in refinishing repaired portions of PCBs. The Pace Kit is an excellent and necessary repair tool wherever piece-part repair takes place; however, it does not contain the equipment required to completely remove and replace conformal coating on a PCB.

The in-circuit tester, commonly called the "bed of nails", is primarily a production line tester. When the PCB is placed in an adapter, as many as 100 or more probes are applied to the board to test each component for its specific value. The major disadvantages of this method are that each type of PCB requires its own rather bulky, complex, and expensive adapter and that the conformal coating must be completely removed from the PCB to ensure that the probes make contact at the many required test points.

The guided-probe method is normally not a stand-alone test method; instead, it is used in conjunction with a fault dictionary to extend the capability of the edge-connector method discussed below. The technician places the probe at a predetermined test point. The fault dictionary, through a display (usually a CRT), directs the technician to the next point on the basis of the tester's determination of a fault or absence of a fault.

In the smart-probe method, a clip is attached to each IC in some predetermined sequence. The clip applies a stimulus to the IC and tests its reaction. The reaction is compared with a fault dictionary table, and a "good" or "bad" indication is obtained. The "bad" indication may direct the next step in the fault-detection/isolation process. This test method can test each IC, and it eliminates the problem of powering PCB (the clip provides the power) and problems associated with adapters. The principal disadvantage associated with it is the requirement to remove and replace the conformal coating on the board.

The edge-connector method tests the PCB through the connector pins on the edge of the board. Most PCBs can be tested by this method; however, as the complexity of PCB circuitry increases, the capability of the tester tends to decrease. This disadvantage can be minimized by using a smart probe or guided probe in combination with the edge tester. For the Army in the field, the edge connector with a guided probe offers the most appropriate test method.

There are two basic types of test patterns, fixed and programmable, that can be used to stimulate the PCB under test. The fixed pattern is the easier of the two for developing a TPS and normally involves lower hardware costs. On the other hand, the programmable patterns allow the programmer to program a bit configuration that most closely resembles the actual input the PCB would encounter in the electronic system. The advantage of programmable patterns over fixed test patterns is offset by several factors:

- A fixed pattern is the least expensive in terms of hardware cost.
- Lower programming skills and less time are required.

- Most fixed patterns can be varied at several different rates; i.e., the DCT becomes a programmable fixed-pattern device.
- A fixed pattern is often adequate to test the PCB, making programmable patterns unnecessary.

Table 3-9 is an overview of the surveyed DCT characteristics associated with fault-detection/isolation techniques. Row 1 indicates the test method, row 2 the types of test patterns, row 3 the maximum test rate, and row 4 the DCT's ability to program the internal power source for the PCB is shown. Rows 5 through 8 are interrelated and are addressed as follows. An indication of a program language in row 5 also indicates a "test only" DCT in row 7. A "test only" DCT requires an external source to generate the test program. The external program source generator device is also listed in row 7. Those DCTs with a large memory capacity (32,000 bits or more) store the "good responses" to a known stimulus for a go/no-go readout on the DCT. The remaining testers make the comparison externally, normally through supporting documentation. Row 8 indicates the number of access pins available on the tester; as a general rule, the DCT with the largest number of pins has the greatest potential test capability.

3.2.3 DCT Categorization

The surveyed DCTs were categorized into three groups, on the basis of their respective test methods and program-generator source, to assist in determining the best set of characteristics for a semi-automatic general purpose digital card tester. The three groups are shown in Table 3-10.

The distinguishing characteristics used to separate the individual DCTs into their respective groups and their application to each group are shown in Table 3-11.

Group 1 DCTs are self-contained units (the 3010A and HC-192 require an external programming panel) that represent the lowest cost to the government while meeting the testing requirements. As a group, they are the least difficult to program; and one of them, the ICT-105, has demonstrated analog capability. Three of these four units have been purchased by DoD activities, and two (the ICT-105 and the HC-192) have been nomenclatured.

Group 2 represents the best test capabilities for a DCT within the constraints of the Summary Table S-1 (with the exception of being programmable in the field and assuming the test-only version for the Data Tester 5800). However, this group has several drawbacks that must be considered. First, extensive external devices such as computers and compilers are required for development of the program portion of the TPS. This will add significantly to the cost of ownership. Second, because of system expansion options and the ability to interface with several different types of peripherals, these DCTs could expand into capability areas reserved for the ATE/ATSS, thus duplicating and not complementing the Army's

Table 3-9. DCT CHARACTERISTICS

Fault-Dection/Isolation Technique	Characteristics by Manufacturer and Model Number									
	Bendix 13A9070	Data Tester 5800	Digital General ELF	Fluke 1000	Fluke 3010A	General Dynamics ICT-105	Hughes HC-192	Mirco Systems 520	Testline 2200	Testline 2300
1. Test Method										
Edge Connector	X	X	X	X	X	X	X	X		
Guided Probe		X	X		X	X	X	X		
Smart Probe		X							X	X
Logic Clip				X	X					
2. Test Pattern										
Fixed	X	X	X	X	X		X	X	X	X
Variable	X	X	X	X	X		X	X	X	X
Programmable		X				X		X		
3. Maximum UUT Test Rate										
Internal (Maximum)	1.25 MHz	400 kHz	5 MHz	4 MHz	4 MHz	4 MHz	4 MHz	Clock Pulse, 700 kHz Pin Change 500 kHz	375 kHz	375 kHz
External Capability	No	Yes	No	No	No	Yes	No	Yes	No	No
4. UUT Power										
Fixed				X					X	X
Programmable	X	X	X		X	X	X	X		
5. Program Language	Mnemonic	Mnemonic	Contest					Mirtest		
6. Memory Capacity (Bits)	32,000	64,000	32,000	0	1,640	0	1,640	32,000	0	0
7. Program Limitations										
Program Generation and Test		X*		X		X			X	X
Test Only	X		X		X		X	X		
Program Source Generator Device	M900		TROLL		3010-592		HC-102A-1	550		
8. Number of Pins	256	256	224	62	192	100	128	224	N/A	N/A

*Only the "Test Only" model is within the constraints of Table S-1.

Table 3-10. DCT GROUPS		
Group 1, Self-Contained Unit	Group 2, Test Only	Group 3, Smart Probe
Fluke 1000A	Bendix 13A9070	Testline 2200
Fluke 3010A	Data Tester 5800	Testline 2300
General Dynamics ICT-105	Data General ELF	
Hughes HC-192	Mirco Systems 520	

Table 3-11. DISTINGUISHING DCT GROUP CHARACTERISTICS

Characteristic	Group 1	Group 2	Group 3
Test Method			
• Edge Connector	×	×	
• Smart Probe			×
Program-Generator Source			
• Internal (Self-Contained)	×		×
• External		×	

planned maintenance structure for the ATS/ATSS. Finally, the requirements for DCT operator skills and TPS development skills are higher -- a difficult factor to quantify in terms of cost although it can be concluded that salaries are higher for more highly skilled employees.

All of the Group 1 and Group 2 DCTs are static test devices; the majority use a test method previously described in this report as an edge connector with a guide probe. This test method is the best fault-detection/isolation method for an Army DCT within the predetermined constraint.

Group 3 represents the "smart probe" test method for fault detection/isolation of a PCB -- the least expensive and probably the best method for fault isolation to a defective IC. However, the "smart probe" cannot quickly determine whether a board is go or no-go. Further, conformal coating must be removed on every suspected PCB before the test begins and, whether or not a fault is detected, the coating must be reapplied. This test method could be useful as a supplement to the ATE/ATSS or as a backup to a go/no-go device that gives reasonable assurance that the PCB to be tested is actually faulty.

The choice of DCT for field activities in the Army should be confined to Group 1 DCTs.

3.2.4 Test Program Sets (TPS)

To develop a TPS for any of the DCTs included in this study, a "known good board" (KGB) and documentation describing its characteristics are required. The KGB and supporting data are analyzed to determine the best methods available to the DCT to stimulate the PCB or KGB. The output responses from the known test patterns are observed and documented and used for subsequent comparisons with suspected PCBs.

The TPS for a DCT consists of three elements: documentation, program source, and interface device/adapter. The TPS cost range depends on the DCT hardware, the fault-detection/isolation technique selected, the program/program source (how progrmming is accomplished), and the level of fault detection/isolation desired. This last factor is further dependent on the level of confidence or test resolution required.

TPS documentation consists of a set of instructions and other information applicable to a specific PCB for use by the DCT operator. Each set of documents is unique to a specific model of PCB and a specific model of DCT, and it is compatible with one program source only. Since the documentation and the test program are unique, they represent the major portion (approximately 80 to 95 percent) of the development cost of a TPS.

The test program consists of a list of instructions to the DCT on which stimuli to apply to the PCB under test, and when and where to apply them. The program may include "known good" stored responses for comparison with the responses of a suspect PCB. The program-generation source or device may be internal or external to the DCT, but in either case the program instructions are transferred to a device that stores the instructions until they are called for to test a PCB. Table 3-12 lists the various TPS program devices used by the DCT manufacturers surveyed.

The interface device or adapter electrically connects the PCB under test to a DCT. In some cases, this device is part of the DCT; in other cases one separate adapter may suffice for all 100-pin PCBs from a particular electronics system. Estimating the cost of interface devices and adapters is difficult without knowledge of the total range of electronic signals on each pin of every PCB in the inventory. However, as a rule, the more flexible a DCT's pin characteristics, the lower the cost associated with interface devices.

Program storage devices and interface devices and adapters, as well as associated documentation, have various life expectancies, depending on usage and storage facilities. The life expectancy of TPSs must therefore be part of the logistics planning process. In addition, as part of the logistics plan, there must be a TPS replacement procedure, as well as a system for identifying TPS faults and modifying TPSs whenever this procedure increases the level of confidence that the program will detect and isolate the fault.

Table 3-12. PROGRAM STORAGE DEVICES

Manufacturer	Model Number	Program Storage Device
Bendix	13A9070	PROM Card
Data Tester	5800	Floppy Disc
Data General	ELF	Tape Cassette
Fluke	1000A 3010A	Performance Board Magnetic Strip on Credit Card
General Dynamics	ICT-105	Plastic IBM Card
Hughes	HC-192	Magnetic Strip on Credit Card
Mirco Systems	520	Tape Cassette
Testline	2200 2300	Floppy Disc Floppy Disc

The TPS is a major factor in the success of a DCT program. To enhance the probability of success, adequate funds must be available for TPS development and testing. Further, a TPS Specification must be available to assist program managers and to ensure that the TPSs are compatible with the Army's selected standard DCT.

3.2.5 TPS Cost, Confidence, and Run-Time Data

Each DCT manufacturer was asked to estimate TPS cost, confidence, and run-time data on a series of hypothetical PCBs and on five actual PCBs currently in the U.S. Army inventory. The results of that portion of the survey are contained in Appendix G. The data in the appendix were used to develop Table 3-13, which indicates the maximum, minimum, and average cost to develop a TPS for the DCT included in each group.

3.2.6 Training

All of the DCT manufacturers surveyed offer several training options at variable cost. They range from "free training" on the operation of a DCT to an estimated high of $10,000 for training on TPS development. The training can be provided at the customer's facility or at the manufacturer's location, with the duration of the training programs seldom exceeding one week.

Table 3-13. TPS ESTIMATED AVERAGE COST BY DCP GROUP			
Level of Fault Detection	Group 1 Costs (Dollars)	Group 2 Costs (Dollars)	Group 3 Costs* (Dollars)
Maximum Fault-Detect/Isolate			
Maximum	1590	5320	158
Minimum	1218	565	158
Average	1408	2223	158
Go/No-Go			
Maximum	1590	3070	158
Minimum	1060	395	158
Average	1323	1578	158

*TPS cost is based on one DCT family of instruments.

Prerequisite skill levels depend on the level of training desired and range from an *unskilled DCT operator* to *a highly skilled technician* or engineer for programming. Training aids are provided to assist in the operation of DCTs and development of TPS.

3.3 DCT MAINTENANCE APPLICATIONS CONCEPT

Forty-four out of 90 DCT Maintenance Applications Concepts Survey Forms were returned to ARINC Research Corporation for review and analysis and the development of a DCT Application Concept. Table 3-14 summarizes the responses to the survey. Of particular interest is the fact that only 28 out of 90 survey participants completed any portion of the form and only 8 made entries in Parts II and III.

3.3.1 Comments on DCT Constraints

There were several comments on the DCT constraints, which are summarized as follows:

- Off-the-shelf should be changed to modified off-the-shelf.
- Field programming of a DCT should be prohibited.
- A level of test confidence should be included.
- The number of equipments making up the test system should be reduced to one, and the weight should be further reduced.

Table 3-14. RESPONSES TO DCT MAINTENANCE APPLICATIONS CONCEPTS SURVEY FORM

Survey Response Category	Number	Percent
1. Survey Forms Distributed	90	100
2. Survey Forms Returned	44	48.9
A. Negative Responses	16	17.8
B. Respondents Completing Part I Only	20	22.2
C. Respondents Completing Parts I and II Only	2	2.2
D. Respondents Completing Parts I and III Only	3	3.3
E. Respondents Completing All Parts	3	3.3
3. Total Number of Survey Responses Evaluated (2B + 2C + 2D + 2E)	28	31.1

- Dollar cost should be lowered to prevent an overlap with Automatic Test Equipment/Automatic Test Support System (ATE/ATSS) capabilities.
- The DCT should complement the ATE/ATSS.

While some of these comments are concerned with policy and thus do not constitute DCT constraints, they are indicative of the role a DCT could play in the Army. They therefore represent a potential framework for subsequent development of a DCT maintenance application concept.

3.3.2 Summary of Responses to the DCT Maintenance Applications Concepts Survey Form

The ability of a DCT to enhance the repair process is recognized, but whether a DCT would reduce the types of TMDE or even the overall quantities of TMDE in the Army has not been clearly established. The need for a device to perform a rapid check of a digital PCB and the trend toward more extensive application of digital circuitry should encourage the search for a standard Army DCT. Such a standard could reduce the number of unique digital TMDE even if there were no corresponding reduction in analog-oriented instruments. It would also help prevent proliferation of this type of TMDE by providing an instrument on which potential users can focus their respective test requirements.

Table 3-15 shows several makes and models of DCTs that have been suggested or noted as on-hand in survey responses. Actual numbers on hand can be found in the survey forms. Of those DCTs addressed in the survey, only the ICT-105 is currently on hand in the U.S. Army. Most of the suggested DCTs are not within the constraints and appear to be in direct competition with large-scale ATE/ATSS. Four of the DCTs are listed in the DA TMDE Register (DA PAM 700-21, January 1977).

Table 3-15. U.S. ARMY SUGGESTED AND ON-HAND DCTs
(Source: DCT Maintenance Concepts Survey)

Manufacturer	Model Number	Suggested DCTs	On Hand	Included in Study	Within Constraints	Not Within Constraints	Listed in DA TMDE Register
Data Test	2000		x			x	x
Fluke	3010A	x		x	x		x
	3020A					x	
	3040A					x	
General Dynamics	ICT-105		x	x	x		
	ICT-103		x		x		x
General Electric	GETS-10	x				x	
GenRad	GR-1792	x				x	x
Hewlett-Packard	DTS-70	x				x	
	9715A	x				x	
Hughes	HC-192	x			x		
	HMP-101	x				x	
Teradyne	L125	x				x	
Testline	1000A	x			x		
	3000A	x				x	

Physical limitations are illustrated in a series of low to high ranges in Part I of Table 3-16. All of the DCTs surveyed fall within these measurement ranges. Part II of Table 3-16 is a comparative illustration of DCT manufacturers' MTBF/MTTR data and U.S. Army requirements for those same DCT characteristics.

Table 3-16. PHYSICAL-LIMITATION RANGES

Part I - Dimensions, Weight, and Environmental	Low	High
1. Dimensions		
Width	15"	36"
Height	8"	36"
Depth	12"	36"
2. Weight	50 lbs	150 lbs
3. Environmental	Class 3	Class 5 (MIL-T-28800B)
	• DS/GS Shop	• Depot
	• A/C Van	• Controlled Environment
Part II - MTBF and MTTR	**DCT Manufacturers**	**U.S. Army Requirements**
4. MTBF	700 to 5000 hrs	250 to 8000 hrs
5. MTTR (Restoral Only)	15 to 30 min	15 to 240 min

Survey results concerning TPS development, control, and modification are shown in Table 3-17. From this table, it is clearly indicated that the prime system manufacturer should develop the TPSs, the commodity manager should control them, and field technicians should not be allowed to program DCTs. The decision for TPS modification, while not as conclusive, slightly favors the depots. The survey results also clearly establish that there is no uniform policy for managing TPS within the Army.

Table 3-17. TPS DEVELOPMENT, CONTROL, AND MODIFICATION

Recommended Source	Best-Case and Worst-Case Situations for TPS Development, Control, and Modification					
	Development		Control		Modification	
	Best	Worst	Best	Worst	Best	Worst
Prime System Manufactured	18	0	2	1	7	10
DCT Manufacturer	4	4	1	4	4	3
U.S. Army Depot	4	4	1	0	8	2
By Contract to a Software House	0	3	0	0	0	1
U.S. Army Technicians in the Field	0	9	1	12	0	10
Commodity Manager	0	0	1	2	0	0
Other	0	0	0	1	1	1

Additional survey responses are recorded in the appropriate spaces in Tables 3-18 through 3-21. They reflect a desire to fault-detect/isolate to the component level with a confidence level of 95 to 99 percent. The test method selected to support these test requirements is the edge connector with a guided probe.

Table 3-18. LEVEL OF FAULT DETECTION/ISOLATION ENVISIONED

Level of Fault Detection/Isolation	Survey Responses	
	Currently Available	Envisioned
Go/No-Go	2	5
Go/No-Go and Circuit (Pin) Isolation Combined	0	3
Go/No-Go, Circuit (Pin), and Component Isolation Combined	0	16

Table 3-19. DESIRED FAULT-DETECTION/ISOLATION LEVEL(S) BY PCB TYPE AND LEVEL

PCB Type	Survey Responses		
	Go/No-Go	Circuit (Pin) Isolation	Component Isolation
Analog	9	5	10
Hybrid	9	4	11
Digital	11	6	13
SSI	8	4	9
MSI	4	6	10
LSI	8	4	8

Table 3-20. LEVEL-OF-CONFIDENCE RESPONSES

Level of Confidence	Survey Responses
Over 99 percent	0
95 to 99 percent	13
90 to 95 percent	9
85 to 90 percent	1

Table 3-21. TEST METHOD(S) SELECTED

Test Method	Survey Responses
Edge Connector	4
Guide Probe	0
Edge Connector with Guide Probe	14
"Smart" Probe	1

There were only four responses to questions related to TPS cost: (1) $350 per TPS, which represented an effort to develop TPSs for the ICT-105 by the U.S. Army Communications Command (USACC); (2) $12,000 per TPS (no DCT was identified); (3) $15,000 per TPS for the EQUATE; and (4) $70,000 per TPS, which was a budget estimate for development of a TPS also on the EQUATE. Except for the USACC figure, the funding requirements anticipated for the development of TPS exceed by many times the actual cost of developing a TPS for any of the DCTs surveyed.

If the U.S. Army had a standard DCT, training on DCT operations should be a part of the training given to personnel in the Military Occupational Specialty (MOS) that supports the major weapon system. Repairs on the DCT should be a responsibility of the Test Equipment Repair MOS. On the basis of foregoing discussions and the survey data, training on the development of TPS should be restricted to the prime weapons system manufacturer and to the depots.

Parts II and III of the survey form contained individualistic and inconclusive data; therefore, the results of those sections in the eight survey forms on which data were entered have been left for ECOM review and possible analysis.

3.4 DESCRIPTION OF THE DCT MAINTENANCE APPLICATION CONCEPT

The majority of the Army survey participants indicated a requirement for fault detection/isolation to the component level. DCTs are capable of performing go/no-go testing and fault detection/isolation to the component level on digital PCBs. However, the confidence level for component testing is lower than the confidence level for go/no-go testing. Further, the cost to develop a TPS increases, as does the level of skill required to operate the DCT and develop the TPS.

Regardless of the effort expended, the PCB can still be tested only under "static test" conditions with a DCT. On the other hand, the ATE/ATSS can provide a "dynamic test" for the PCB, thus increasing chances (level of confidence) that all faults (catastrophic and marginal) are detected, isolated, and corrected. Therefore, since fault detection/isolation to the component level is the planned maintenance concept for the ATE/ATSS, it appears injudicious to attempt to make the DCT match this test capability. (The difference between "static test" and "dynamic test" was discussed in Section 3.2.2.)

There are, as always, valid exceptions; e.g., the TPSs for a low-density electronic system that will be isolated and will require on-site repair should include the capability to fault-isolate to the component level with a DCT. This decision must be made by the program manager during the development of electronic systems.

The DCT role should be twofold:

- The DCT should test PCBs for a go/no-go indication before they are submitted for replacement or repair.
- The DCT should be able to fault-detect and fault-isolate to the component level whenever the density and planned deployment of the electronic system warrants.

Under the maintenance application concept of a go/no-go tester, the DCT would act as a screening device, with the primary objective of reducing the number of good PCBs being sent into the repair process. On the less complex PCBs it would also provide a quality-assurance function by verifying workmanship, i.e., determining that there are no shorts or opens on the repaired PCB.

Expanding the maintenance application concept of the Army's DCT to include fault detection/isolation to the component level should be restricted to small-population electronic systems that are deployed in isolated locations and must be repaired on site. However, since the DCT can provide only static testing, it might be more feasible to increase the number of spare PCBs than to attempt fault isolation with the DCT. Further, the level of confidence may be too low and therefore create as many maintenance problems as it solves.

To meet the DCT Maintenance Application Concept described above, the Army Standard DCT must have the capability to perform go/no-go testing on a wide variety of PCBs. It should also be able to fault-isolate to the component level for special applications, as discussed above.

3.5 DETERMINING THE DCT PARAMETERS

The determination of the DCT parameters for the Army Standard DCT is closely related to intended maintenance applications envisioned for this instrument. The recommended role is that of a go/no-go tester, with a minor role of fault isolation to the component level -- the latter being confined to unique situations such as small-population electronic systems that are deployed in remote locations. The Group 1 DCTs contain the necessary test capability to meet the requirements of this recommended maintenance application concept.

Opting for the Group 1 DCTs would establish them as the starting point for the development of the Army Standard DCT procurement specification. This decision would involve the lowest initial cost. It would also reduce the total cost of ownership, primarily because the logistics costs associated with the external program-generating devices required by the Group 2 "test only" DCTs are eliminated and the costs of TPS and training are significantly reduced.

Conversely, the decision to opt for a maximum fault-detection/isolation test capability by the selection of the Group 2 "test only" category of DCT would increase initial cost, total cost of ownership, and TPS cost. The cost relationships are illustrated by Figure 3-2.

The level of fault detection/isolation desired in an Army Standard DCT will be reflected in the cost, skills, and time necessary to develop the appropriate TPS. Figure 3-2 amplifies this point. This figure is derived from the average cost of a TPS as compiled in Appendix G (Table G-8, Parts I and II) and technical journals and publications listed in Appendix A. It shows that as the complexity of the PCB increases, software cost, time, and operator skills must increase. A portion of the skill-level requirements can be traded off by increasing the test system capabilities, but the trade-off will probably not significantly reduce the cost of the TPS software and the time required to develop it.

The test capability of each DCT can be defined as the number and types of test patterns, rates, pins, and machine/operator interfaces, as well as TPS development requirements. It can be expressed in dollars -- the higher the cost the greater the capabilities. A unit cost difference of $1,000 to $5,000 is probably not important. However, a unit cost difference of more

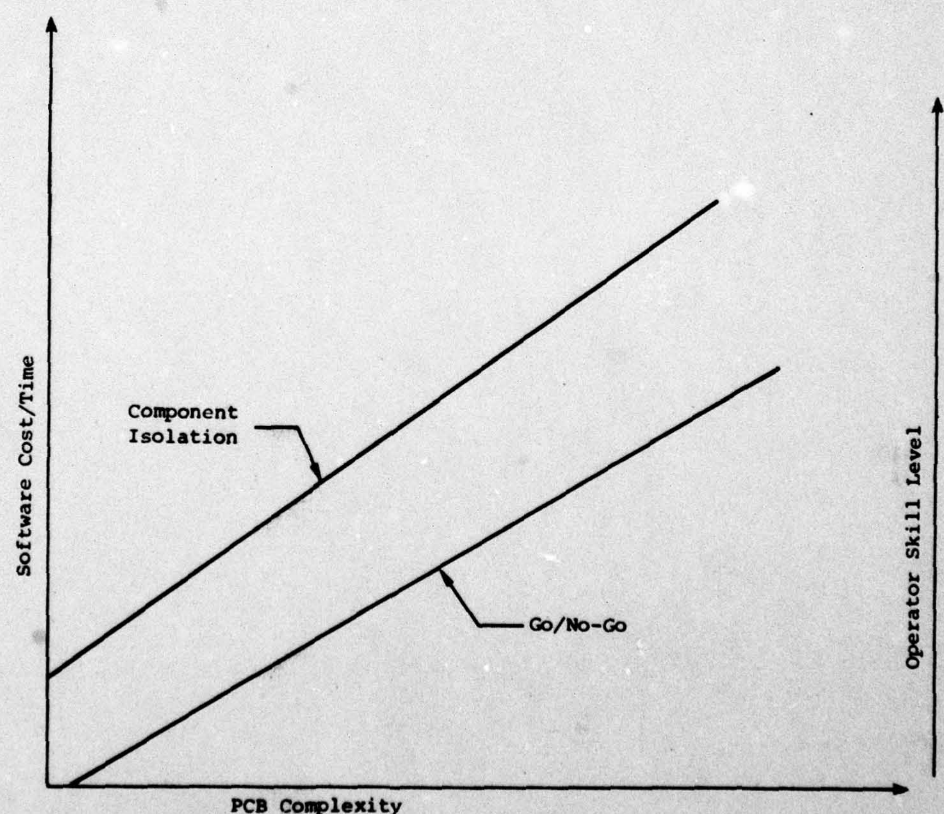

Figure 3-2. PCB COMPLEXITY/SOFTWARE COST

than $5,000 between DCTs would imply some capability differences that may be significant. Further, the total cost of ownership (life-cycle cost) must be considered in any final selection of a DCT.

Group 1 testers are the least expensive (average cost: $13,628), and they could complement the ATE/ATSS; but they have less test capability. On the other hand, the Group 2 testers are the most expensive (average cost: $30,982), and they would be in competition with the ATE/ATSS because they have the greater test capability.

CHAPTER FOUR

CONCLUSIONS AND RECOMMENDATIONS

4.1 CONCLUSIONS

The information contained in the DCT Maintenance Application Concepts Survey form suggests that there is a requirement for an Army Standard DCT. However, this requirement has not been quantified, it is therefore difficult to determine the period in which the Army Standard DCT must be made available to prevent proliferation of this type of instrument. Table 3-15 provides an indication of activities in this area.

The application potential of a DCT is recognized, and several program managers indicated a willingness to explore the applications of a DCT in support of their system. It can be assumed that additional activities would explore the DCTs potential if it were available. Further, since the trend in electronics is toward digital PCBs, the existence of an Army Standard DCT would prevent future proliferation in this category of TMDE.

The DCT constraints should be adjusted to reflect those shown in Table 4-1. These constraints more closely reflect the Group 1 DCTs and U.S. Army requirements for a DCT.

Table 4-1. RECOMMENDED DCT CONSTRAINTS
• The DCT must be procurable modified off-the-shelf (OTS).
• The DCT must be portable and capable of operating from either 50/60 or 400 Hz 115/230 Vac power sources. (The DCT can be modified to meet this constraint.)
• The DCT must not exceed two separate units, exclusive of program files, accessories, and external test equipment.
• The total weight of the DCT must not exceed 100 pounds (45.36 kilograms), with no individual unit exceeding 90 pounds (40.82 kilograms).
• The cost of each DCT system (less TPS cost) must not exceed $20,000.
• The average cost of TPS set should not exceed $2,000.
• The level of confidence should be 95 percent or better for all TPS.

The "Best Set of Characteristics for a General Purpose Digital Card Tester", presented in Appendix H, is derived from the Group 1 (self-contained units) listed in Table 3-28. The Group 1 DCTs have the test capability requirements to meet the DCT Maintenance Application Concept discussed in Section 3.5. This concept establishes the maintenance role of a DCT as primarily that of a go/no-go tester with the objective of reducing the number of good PCBs placed into the repair processes. A secondary role of fault detection/isolation to the component level is included in the DCT Maintenance Application Concept, for small-population electronic systems deployed in remote locations.

The hardware/software cost data for a DCT are summarized in Table 4-2, which indicates the low and high ranges for one unit, as well as for that unit expanded to its maximum test capability by the addition of the various options previously noted in Table 3-5.

Table 4-2. HARDWARE/SOFTWARE BASIC COST DATA (In Dollars)

Hardware/Software Category	Range		Remarks
	Low	High	
Digital Card Tester			
Unit Cost	7400	39,950	
Expanded Test System Cost	7870	52,300	
Documentation (Support Manuals	0	25	Includes schematics and parts list
Spares Kits	Unknown	8,600	Includes spare modules and piece parts
Training	Free	10,000	Depends on level of training desired
Total			
DCT (Unit) and Training	7400	58,572	
DCT (Expanded System) and Training	7870	70,925	

Total investment (less TPS) for a Group 1 DCT will not exceed $30,000, including the "expanded system", documentation, training (at the manufacturer's facility for one week), and a spare-modules/repair-parts kit.

The elements that make up a TPS have various life expectancies, depending on usage and storage conditions. Their life expectancy must therefore be considered in the logistics planning process and a replacement system devised. Further, adequate funds for TPS development and testing must be available to enhance the probability of success.

As a member of the TMDE family, the DCT must fill a void in the existing and planned Army maintenance structure for Army support equipment -- that is, the advantages of a DCT in support of the mission equipment must exceed the disadvantages of supporting another piece of support equipment in the field.

4.2 RECOMMENDATIONS

ECOM should proceed with the preparation of a DCT specification for an Army Standard DCT. This instrument should conform to the DCT characteristics as portrayed by the DCTs listed in Table 3-20 under Group 1 and reflected in Appendix H.

The requirements for an Army DCT should be further qualified and quantified both in the short term and in the long term. The procurement of the Army Standard DCT should be a coordinated effort with the ATE/ATSS program to ensure that the DCT complements this program and conforms to the Army's future maintenance structure. The procurement strategy should include determination and verification of the testability of a variety of PCBs on the competing testers.

As a part of the overall DCT program, a "DCT Applications Planning Guide" should be developed around the standard DCT to assist program managers and other activities in determining whether the DCT should be a part of their support system.

As a section of the planning guide, a detailed TPS specification should be developed and a TPS management program established within the Army. A TPS specification would ensure uniformity and compatibility with the standard DCT and provide a method for determining TPS cost and test resolutions for a group of PCBs related to a specific end item. The management system would delegate responsibility for the development, maintenance, modification, and overall control of the TPSs.

<u>Note</u>: The conclusions and recommendations contained in this report are in part based on a very limited number of responses from the U.S. Army survey participants.

APPENDIX A

TECHNICAL JOURNALS AND PUBLICATIONS

1. E. A. Torrero, "ATE: Not so Easy", *IEEE Spectrum*, April 1977.

2. M. Elecion, "Automatic Test Equipment Hardware and Software", *IEEE Spectrum*, June 1976.

3. H. W. Markstein, "Packaging for the Military Environment", *Electronic Packaging and Production*, February 1977.

4. "Multiple Probe Fixtures", *Circuits Manufacturing*, March 1976.

5. G. King, "In-Circuit Testers Find Faults Fast in Populated Boards", *Electronic Packaging and Production*, February 1977.

6. "Compare the Programming Aids Offered by Different ATE Makers", *Evaluation Engineering*, May/June 1977.

7. R. Seltzer, "Test Strategies", *Circuits Manufacturing*, January 1977.

8. R. E. Tulloss, "Automatic Test Systems", *IEEE Spectrum*, September 1974.

9. G. Voget, "Taming the RAMS", *Circuits Manufacturing*, December 1976.

10. G. King, "Comparison Testers Can Check all Members of Microprocessor Family Logically, Electrically," *Electronic Packaging and Production*, January 1977.

11. G. R. Welden, "Removing Conformal Costings Facilitates Electrical Testing", *Circuits Manufacturing*, December 1976.

12. S. Holyfield, "Testing: What the Future Holds", *Electronic Packaging and Production*, January 1976.

13. Electro 77 Professional Program - April 1977

    - "Predicting Test Effectiveness on Assembled PCBs", No. 18.
    - "Testing Microprocessors on Boards", No. 25.
    - "Testing Complex Digital Assemblies", No. 32.
    - "Serviceability and Maintainability in the Product Planning Equation", No. 11.

14. H. P. Hall, "Analog Tests: The Microprocessor Scores", *IEEE Spectrum*, 1977.

15. A. Santoni, "Digital Systems Spawn New Tasks in Measurements", *Electronics*, October 1976.

16. "Test Equipment and Services Reference", *Evaluation Engineering*, July/August 1976.

17. J. A. Barnshaw, "Evaluating a Diagnostic Program", May 1977.

18. "100% Testing Cuts Costs," *Quality*, May 1977.

19. "Bench Top Testers for 1976", *Evaluation Engineering*, January/February 1976.

20. E. Riddel, "Programmable Logic Board Testers", *Circuits Manufacturing*, June 1976.

21. C. T. Pynn, "In-Circuit Inspection Testing: The New Generation", *Evaluation Engineering*, July/August 1977.

22. J. Redditt, "Minimizing Set-Up Costs for ATE", *Electronic Packaging and Production*, July 1977.

23. H. K. Dicken, "What Can Happen to an IC In Your System?", *Evaluation Engineering*, July/August 1977.

24. R. L. Petritz, "The Pervasive Microprocessor: Trends and Prospects", *IEEE Spectrum*, July 1977.

APPENDIX B

ARINC
A Subsidiary of Aeronautical Radio, Inc.

May 31, 1977
DC^{3}G/TSP-77-101
Contract DAEA 18-72-A-0005
Work Order 1073-04

Reply to Code DC^{3}G

Attention: Director of Marketing

Subject: Digital Card Tester Characteristics

Dear Sir:

ARINC Research Corporation was recently awarded a six-month contract (DAEA 18-72-A-0005) to assist the U. S. Army Electronics Command (ECOM) in determining the best set of characteristics for a general purpose semi-automatic Digital Card Tester (DCT) that meets U. S. Army testing requirements. The Program is being planned and administered by the TMDE Division of the Directorate of Maintenance and is directed at the eventual competitive procurement of a commercial Off-the-Shelf (OTS) Digital Card Tester. The thrust of the study is to facilitate greater use by the Army of commercially available Electronic Test Equipment (ETE).

The ARINC Research project consists of several tasks starting with an evaluation of the Semi-Automatic General Purpose Digital Card Tester Market and ending with the preparation of parameters for a DCT. The initial effort is directed at a review of the technological trends of the DCT industry and the selection of up to 20 DCTs by manufacturers' model number for a further in-depth analysis.

In our efforts to identify 20 DCTs, your company's name has surfaced as a potential source. This information was obtained from the magazine "Circuit Manufacturing", dated January 1977. You can assist this corporation in meeting the objectives of the study <u>by providing, no later than 15 June, current literature that describes your product line of Digital Card Testers</u> that fall within or near the constraints listed below:

Phone: Annapolis 301-224-4000 Washington, D. C. 261-8100 Santa Ana, Calif. 714-547-7504 TWX: Annapolis 710-867-9663 Santa Ana, Calif. 910-595-1110

- Must be portable/mobile
- Must not exceed more than three separate units not to include program files, accessories, etc.
- Must not exceed 200 pounds total weight, with no one individual unit to exceed 95 pounds.
- Cost less than $100K.
- Must be programmable, in the field, by a skilled electronics repair technician.

The above constraints should not be considered as "final", but representative of the initial "thinking" by U. S. Army and ARINC Research personnel. In addition, any technological trend data you could provide would be greatly appreciated. Should you have any questions, the ARINC Research Corporation point of contact is Mr. A. Simmons, (301) 224-4000, extension 369.

It should be understood that this letter, or any future correspondence relating to the program, does not in any way obligate either the U. S. Army or ARINC Research Corporation to either purchase any specific product or compensate you in any way for any services or assistance offered or solicited. Finally, should you elect to contribute information to the effort which you consider to be proprietary, you can be assured that such information will be appropriately protected in accordance with your wishes.

An early response would be greatly appreciated.

Very truly yours,

Larry J. Graham

Larry J. Graham
Project Engineer

LJG/ALS/SEG

ARINC
2551 Riva Road • Annapolis, Maryland 21401

July 14, 1977
DC3G/TSP-77-140
Contract DAEA 18-72-A-0005
Work Order 1073-04

Attention:

Subject: Digital Card Tester Characteristics

Dear Sir:

ARINC Research Corporation, a consulting and engineering research company, was recently awarded a six-month contract (DAEA 18-72-A-0005) to assist the U.S. Army Electronics Command (ECOM) in determining the best set of characteristics for a general-purpose semi-automatic Digital Card Tester (DCT) that meets U.S. Army testing requirements. The program is being planned and administered by the TMDE Division of the Directorate of Maintenance and is directed at the eventual competitive procurement of a commercial Off-the-Shelf (OTS) Digital Card Tester. The goal of the study is to facilitate greater use by the Army of commercially available Electronic Test Equipment (ETE).

The ARINC Research project in support of this program consists of several tasks, starting with an evaluation of the Semi-Automatic General Purpose Digital Card Tester market and ending with the identification of parameters for a DCT. The initial effort was directed at a review of the technological trends of the DCT industry and the selection of up to 20 DCTs for further analysis. This process has resulted in the selection of your company's DCT model number

The present task in the DCT project is to obtain data from the manufacturers of the selected DCTs that will enable us to establish DCT characteristics, capabilities, and cost figures for subsequent analysis. You can assist in meeting the objectives of this U.S. Army program by completing and returning the "Digital Card Tester (DCT) Capabilities Survey" form attached as an enclosure to this letter.

Phones: Annapolis 301-224-4000 Washington, D. C. 261-8100 Santa Ana, Calif. 714-547-7904 TWX: Annapolis 710-867-9663 Santa Ana, Calif. 910-595-1110

The survey has a two-fold purpose: to provide information on the U.S. Army's DCT program, and to request information from the manufacturers of this type of equipment. It further allows for the provision of supplemental information at your discretion.

Because of the time constraints of the contract, the completed survey form and supporting data must be received by ARINC Research Corporation no later than August 19, 1977. Responses received after that date cannot be considered.

Since the basic purpose of this survey is to obtain information from the selected manufacturers for the U.S. Army study program described above, it should be understood that neither this letter, nor any future correspondence relating to the program, in any way obligates the U.S. Army or ARINC Research Corporation to purchase any product from the manufacturers or to compensate them in any way for any services or assistance offered or solicited.

An early response would be greatly appreciated.

Very truly yours,

Larry J. Graham

Larry J. Graham
Project Engineer

DIGITAL CARD TESTER (DCT)

CAPABILITIES SURVEY

July 1977

Prepared by

A. L. Simmons

ARINC Research Corporation
a Subsidiary of Aeronautical Radio, Inc.
2551 Riva Road
Annapolis, Maryland 21401

CONTENTS

INTRODUCTION

The Digital Card Tester (DCT) Capabilities Survey Sheet is intended to provide information to the U.S. Army Electronics Command (ECOM) for use in determining the set of DCT characteristics and test methodology which can best meet the digital test requirements of U.S. Army electronic systems, both currently fielded and planned. Cost data on the DCT equipment, accessories, and support items, to include Test Program Sets (TPSs), are included in the survey to provide ECOM with a range of "cost vs characteristics" for subsequent trade-off analysis.

The information provided is expected to lead to the development of a military specification for the competitive procurement of an off-the-shelf (OTS) general-purpose DCT for support of U.S. Army electronic systems.

If, in your opinion, the surveyed data elements leave "gaps" in DCT technology, cost data, etc., please feel free to supplement existing elements, to add new elements, and to provide supporting materials. Further, if the space provided for answers is inadequate, please attach additional sheets to the survey form. Finally, the answers to the survey questions for your equipment as described in Paragraph 1.0 should be for that unit at its maximum test capability. That is, if your equipment features a range of options (e.g., a fixed pattern vs. a programmable pattern) that extends the equipment's functional capabilities, the maximum functional capability options should be described in your answers.

The completed survey document will be forwarded to ECOM approximately November 8, 1977, and at that time the remaining materials provided will be returned to your company or otherwise disposed of in accordance with your instructions.

If you have questions concerning the intent of the DCT program or this survey sheet, please call either of the following representatives of ARINC Research Corporation, Annapolis, Maryland:

Mr. Albert L. Simmons - (301) 224-4000, ext. 369

Mr. Larry J. Graham - (301) 224-4000, ext. 400

DIGITAL CARD TESTER (DCT) CONSTRAINTS

The following "contraints" were part of the criteria by which DCT equipment was selected for this survey. The answers and supporting data which you provide concerning your equipment should be within the boundaries of these constraints.

- The DCT must be procurable off-the-shelf (OTS).
- The DCT must be portable and capable of operating from either a 50/60 or 400 Hz, 115/230 Vac power source. (The DCTs can be modified to meet this constraint.)

- The DCT must not exceed three separate units, exclusive of program files, accessories, and external test equipment.
- The total weight of the DCT must not exceed 200 pounds (90.72 kilograms), with no individual unit exceeding 95 pounds (43.1 kilograms).
- The cost of each DCT system (less TPS cost) must not exceed $50,000.
- The DCT must be programmable, in the field, by a skilled electronics repair technician.

These constraints should not be considered final; they represent the views of U.S. Army and ARINC Research Corporation personnel at the current stage of the DCT characteristics study.

1.0 Equipment Description

1.1 This survey sheet pertains to the Digital Card Tester (DCT) Model Number ____________ manufactured by ____________ and all questions herein are related to that equipment item and no other.

1.1.1 Describe options/features applicable to the DCT model above that are within the "Constraints" and extend the DCT to the maximum test capabilities: ____________

____

____

____

1.2 Date (Month/Year) the equipment was first offered on the commercial market ____________

1.3 Is the equipment an improved version over any previous model(s) offered by your company? Yes____ No____

1.3.1 If yes, please list the previous model(s):

____

____

____

1.4 Please complete as applicable. The following point(s) of contact are available to ARINC Research Corporation and Government personnel to answer questions pertaining to the equipment:

Name and Title	Area Code and Phone No./Ext.	Area(s) of Expertise

2.0 General

2.1 To ensure that your equipment receives a complete and accurate evaluation, it is requested that you provide the type(s) of publication(s) listed below. (Provision of publications must be at no cost to ARINC Research Corporation or to the U.S. Government. All publications provided will be returned to your company or disposed of per your instructions, at the close of the survey program, i.e., approximately 8 November 1977).

2.1.1 Equipment publications that describe the following:

- Technical Characteristics
- Operator Procedures, Controls, etc.
- System Architecture
- Theory of Operation
- Maintenance Procedures, including:
  - •• Schematics
  - •• Illustrated Parts Breakout
  - •• Parts List
- Calibration Procedures and Interval
- Programming Procedures, including Material Requirement

2.1.2 GSA schedule or current price list (includes cost of basic unit, accessories, options, programming materials).

2.1.3 Brochures, etc., that describe options or other related technical capabilities data.

2.1.4 An equipment training course outline for the following:

- Operation of the equipment
- Maintenance of the equipment
- TPS development and validation

2.1.5 The requested publication(s) are enclosed except for the items circuled above. Yes____No____

2.1.6 Portions of this survey form can be completed by ARINC Research Corporation personnel from the data requested above, as noted throughout the form. However, to avoid misunderstanding, you should review each question to ensure that the answers are included in the publications you provide. Further, you should note the source document and page number next to the questions to assure an accurate and complete evaluation of the equipment.

2.2 The eventual procurement of a Digital Card Tester (DCT) by the U.S. Army is intended to be in accordance with MIL-T-28800B. This specification describes the general requirements for test equipment used in testing electrical and electronic equipment. Within this specification the various types, classes, styles, and colors for test equipment are outlined. The intended procurement is for an equipment of Type III, Class 5, Styles E and F, and Color R. These categories are defined in MIL-T-28800B as follows:

- Type III. Type III equipments are those commercial off-the-shelf equipments which meet specific military requirements as described herein.
- Class 5. Test equipments for use as a bench-top or rackmounted instrument, designed for use in a fixed location and not requiring integral protection against exposure. Equipments of this class will normally be designed with enclosures of Style E or F (0°C to 50°C).
- Style E enclosure (equipment case). Enclosures of this style will provide minimal protection from mechanical shock or falling water particles. Protection for the instrument may be restricted to bench handling and use. Equipments with enclosures of this style are normally used in an environmentally controlled area. These enclosures are an integral part of the equipment.
- Style F enclosure (rackmount case). Enclosures of this style are designed for rackmounting without the use of a conversion kit. This style enclosure is normally contained in a Style G console cabinet. These enclosures are an integral part of the equipment.
- Color R. Other (color as normally provided by the manufacturer or as required in the detailed specification).

The power source requirements for Type III test equipment are:

50, 60 and 400 Hz, 115 Vac/230 Vac single phase.

2.2.1 Is your company familiar with MIL-T-28800B? Yes____No____

2.2.2 Has the make/model of equipment described in Paragraph 1.0 been purchased within the last year by any element in the Department of Defense (DoD)? Yes____No____

If yes, please complete the following (the point-of-contact refers to the actual user of the DCT and not the purchasing activity):

Agency	Quantity	Date Purchased	Point-of-Contact in DoD

2.2.3 Are you aware of any Joint Electronics Type Designator (JETD) or national stock number (NSN) having been assigned by any of the above DoD agencies? Yes____No____

If yes, please complete the following:

Agency	JETDS	NSN

2.2.4 Did any of the DoD agencies require your company to revise the equipment manual into a "Military Standard" format or did they "overprint" it with a military publication number? Yes____No____

If yes, please complete the following:

Agency	DoD Pub. Number (if known)	Remarks

3.0 COST

3.1 Is the equipment listed in the General Services Administration (GSA) schedule? Yes___No____

3.1.1 If yes, please list the contract number and the effective date:

____

3.1.2 Or enclose a copy of the GSA schedule. Copy enclosed? Yes___No____

NOTE: If a GSA schedule or price list is enclosed, the remainder of Section 3 can be completed by ARINC Research Corporation, except for paragraph 3.7.

3.2 Equipment Cost (enter single unit cost in space provided).

3.2.1 Equipment in Bench-Top Configuration: $__________

3.2.2 Equipment in Rackmount Configuration: $__________

3.2.3 Equipment Option(s).

Part Number	Description	Cost	Remarks

3.3 Accessories Cost (enter single unit cost in space provided):

Part Number	Description	Cost	Remarks

3.4 Programming Materials (e.g., worksheets, diagrams, tables, etc.) (enter cost data in space provided):

Part Number	Description	Cost	Remarks

3.5 Technical Publications (enter single-unit cost in space provided)

Part Number	Description, including:	Cost	Remarks
	Operator:		
	Maintenance:		
	Programming:		
	Others:		

3.6 Repair/Spares Kit (enter the single-unit cost). Additional questions related to support of the equipment are contained in Paragraph 6.0.

Part Number	Description	Cost	Remarks

3.7 Training. Describe the training course(s), including cost, that your company would provide to commercial customers for the equipment. Additional questions related to training on the equipment are contained in Paragraph 8.0. (Attach supporting material as required).

____

____

____

4.0 Operational Capabilities

4.1 Technical Characteristics. Describe and/or attach parameter sheets as necessary.

NOTE: Paragraph 4.1 can be completed by ARINC Research Corporation personnel from the publications requested in Paragraph 2.1. Please note the reference source(s) and page number(s) after each question.

4.1.1 Diagnostic Methodology

- Interface device(s): DCT to PCB

4.1.2 Programming Language

4.1.3 Maximum program size allowed (without external devices).

4.1.4 Clock Speed/Frequency

- Internal
- External

4.1.5 Stimulus - How many?

- Fixed
- Programmable

4.1.6 Test Voltages - How many?

- Fixed
- Programmable
- Voltage level(s) and power capacity

4.1.7 Pin Characteristics

- Number
- Direct/Bi-directional

4.1.8 Self-Test Capability

4.1.9 Operator Interface

4.2 Is external test equipment required in conjunction with the equipment? Yes____ No____

4.2.1 If yes, please describe the types and technical parameters.

____

____

____

4.2.2 List recommended test equipment by manufacturer's model number.

Type	Manufacturer	Model No.	Remarks

4.2.2.1 Does the above-recommended test equipment supplement the DCT equipment and/or extend its operational capabilities? Please describe:

____

____

____

4.3 Below is an applications summary matrix which is intended to correlate the types of PCBs to the "Fault detection/isolation" level capabilities of the equipment. The following assumptions are made: the hybrid PCB contains 10 MSI ICs, the SSI PCB contains 50 ICs, the MSI PCB contains 25 ICs, and the LSI PCB contains 5 ICs. All PCBs have 200-pin edge connectors. Correlate and enter the estimated equipment run time to fault-isolate to the indicated level.

TYPES OF PCB

Level of Fault Detection/ Isolation	Hybrid	SSI	MSI	LSI	Remarks
Go/No-Go	____	____	____	____	____
Circuit (PIN)	____	____	____	____	____
Component	____	____	____	____	____

Comments:____

____

____

____

4.4 Is the equipment capable of performing an end-to-end test on a <u>Line Replaceable Unit (LRU)</u> and fault-isolate to a defective printed circuit board? Yes____ No____

4.4.1 If yes, please describe this capability and its limitations:______

____

____

____

4.5 Is the equipment capable of performing a Go/No-Go check of an analog PCB? Yes____ No____ Comment:_____________________________________

____

____

____

5.0 Physical

5.1 Dimensions and weight: State the maximum dimensions (height, width, depth) and weight in metric units for the equipment for the two types of enclosures described below:

5.1.1 Style E Enclosure (Equipment Case)

Height:____________________cm

Width:____________________cm

Depth:____________________cm

Weight:____________________kg

5.1.2 Style F Enclosure (Rackmount Case)

Height:____________________cm

Width:____________________cm

Depth:____________________cm

Weight:____________________kg

5.2 Power consumption: State the maximum power consumed by the equipment: ________________ watts.

5.2.1 If the equipment can be operated from a dc battery source, state the battery size, complement, operating life/recharge time:____________

____

____

____

5.3 Power source: Can the equipment operate from a 50/60 or 400 Hz 115/230 Vac power source? Yes____No____

5.3.1 If no, state limitations:________________________________

____

____

____

5.3.2 Can the equipment be modified to meet these requirements? Yes____No____

5.4 Describe the type of construction; i.e., modular, solid state, etc.

____

____

____

5.5 Describe the environmental limitations of the equipment:

5.5.1 Temperature range

Operating: ____________

Nonoperating: ____________

5.5.2 Relative Humidity: ____________

5.5.3 Altitude:

Operating: ____________

Nonoperating: ____________

5.5.4 Vibration limits: ____________

5.5.5 Fungus Resistance: ____________

5.5.6 Others as applicable: ____

____

____

6.0 Support

6.1 Documentation: This portion of Section 6 includes an evaluation of the equipment's supporting documentation (i.e., operator, maintenance, and programming manuals) by ARINC Research; it can be completed only from the documents requested in Paragraph 2.1. The intent is to review the documents for clarity and completeness.

6.2 Reliability: Indicate the reliability in terms of Mean Time Between Failures (MTBF) expressed in hours of continuous operation. Next to the space labeled "History", indicate the MTBF as derived from historical operational data. Next to the space labeled "Prediction", indicate the MTBF from a parts-count reliability prediction: (IAW MIL-Handbook-217B).

History ____

Prediction ____

6.3 Maintainability: Indicate the maintainability in terms of Mean Time to Repair (MTTR) expressed in hours/minutes. Next to the space labeled "Restoral" indicate the time required to troubleshoot and restore the DCT to an operational mode. Next to the space labeled "Repair" indicate the time required to fault-isolate and repair a faulty component. (assume parts are available).

Restoral ____

Repair ____

6.4 Does your company have a "recommended" logistics support system for the equipment? Yes____No____

6.4.1 If yes, describe the support system:______________________________

____

____

____

6.4.1.1 Does the support system include: (✓ where appropriate)

- Spares Kit ______
  - Spare Modules for the equipment ______
  - Repair Parts ______
- Repair Services ______
  - Field ______
  - In-Plant ______

6.5 Are any of the piece parts or equipment accessories procurable only through your company? Yes____No____ Comment:______________________

____

____

____

6.6 Does the equipment require calibration other than self-calibration? Yes____No____

6.6.1 If yes, what is the calibration interval?______________________

____

____

6.6.2 Are there any "special" calibration equipment or fixtures required that are available only at your facility? Yes____No____

6.6.2.1 If yes, please describe:______________________________

____

____

____

6.7 Describe the "warranty" you would provide with the sale of the equipment to a commercial customer:______________________________

____

____

7.0 Test Program Set (TPS)

This section is related to the documentation provided in Appendixes A through E for five (5) printed circuit boards (PCBs) which are found within the U.S. Army equipment inventory. The PCB documentation includes the following:

- Schematic
- Theory of Operation
- Illustrated Parts Breakout
- Parts List

7.1 Based on the 5 document packages, could your company estimate the cost of developing a TPS for each of the boards that would "run" on the equipment? Yes____No____ Comment:______________________________

____

____

____

7.1.1 If the answer to 7.1.1 is "no", please indicate one of the following with a √ mark.

7.1.1.1 ☐ TPS cost can be estimated, but the following additional documentation(s) is/are required to ensure quality results:______________________________

____

7.1.1.2 ☐ TPS cost cannot be estimated without the following additional documentation:____________________

____

7.2 Assuming the 5 PCBs are programmable, to what level(s) of fault detection/isolation can each PCB be programmed? Check all levels in the appropriate space provided in the matrix.

Level of Fault Detection/Isolation	PCB Described in Appendixes A	B	C	D	E
Go/No-Go	____	____	____	____	____
Circuit Isolation	____	____	____	____	____
Component Isolation	____	____	____	____	____

7.3 If the cost to develop a TPS for each of the PCBs can be estimated, please complete the following matrix by entering the appropriate cost data (in $) correlated to the maximum level of fault detection/isolation obtainable, as indicated in Paragraph 7.2.

Test Program Set (TPS) Cost	PCBs Described in Appendixes				
	A	B	C	D	E
Documentation Cost	____	____	____	____	____
Interface Device Cost	____	____	____	____	____
Programming Cost	____	____	____	____	____
Others (describe) Cost	____	____	____	____	____
Total Cost	____	____	____	____	____

7.3.1 Assuming your customer required two (2) copies of each TPS, enter the cost of duplicating each of the above TPSs.

Appendix	Duplication Cost
A	____
B	____
C	____
D	____
E	____

7.3.2 Assuming your customer requested the 5 PCBs to be programmed for a Go/No-Go indication only, please estimate and enter the cost data (in $) for each of the elements in a TPS:

Test Program Set (TPS) Cost	PCBs Described in Appendixes				
	A	B	C	D	E
Document Cost	____	____	____	____	____
Interface Device Cost	____	____	____	____	____
Programming Cost	____	____	____	____	____
Others (describe) Cost	____	____	____	____	____
Total Cost	____	____	____	____	____

7.4 Have you established any guidelines for determining/estimating an expected level of test confidence for a TPS? Yes____ No____

7.4.1 If yes, please elaborate:______________________________

____

____

7.4.2 If yes, please indicate the level of confidence for each of the potential TPSs in Paragraphs 7.3 and 7.3.2.

	7.3	7.3.2
Appendix A:	________	________
Appendix B:	________	________
Appendix C:	________	________
Appendix D:	________	________
Appendix E:	________	________

7.5 What are the estimated "run times" for each of the TPSs listed in Paragraphs 7.3 and 7.3.2?

	7.3	7.3.2
Appendix A:	________	________
Appendix B:	________	________
Appendix C:	________	________
Appendix D:	________	________
Appendix E:	________	________

8.0 Training

The questions in this section relate to the services your company might provide to a non-government purchaser of the equipment.

8.1 Does your company provide training on the equipment? Yes____ No____

8.1.1 If yes, please ✓ the type of training and indicate the estimated duration.

Type of Training	Duration
______ Operator	________
______ Maintenance of DCT	________
______ Programming TPS for DCT	________

8.1.2 Is the training provided: (Please ✓ appropriate spaces)

In-Plant only ______

Customer's facility only ______

Both of the above ______

8.2 Describe the "Prerequisite Skill Level" required by your company for each of the training levels indicated below:

8.2.1 Operator: ____

8.2.2 Maintenance of DCT: __________________________________

8.2.3 Programming TPS for DCT: ______________________________

8.3 Can you provide documented experience of your training success on the equipment if requested by the U.S. Army? Yes____ No____

8.4 Programming Aids: Describe the programming aids that are required/ available for the development of TPS: ____________________________

This completes the survey. Thank you for your participation and cooperation.

APPENDIX A

DISTORTION GATE GENERATOR 1A2A6
(FIGURE 6-23)

Assembly 1A2A6 contains the divide-by-2 flip-flop, dual decade, units and tens combiners and a clock output flip-flop. An input frequency at 200 times the baud rate from 1A2A11 is applied to inverter Z4I1. Flip-flop Z1FF1 divides the output of Z4I1 by 2 and presents the ones decade with an input frequency of 100 times the baud rate. The output of the ones decade provides the tens decade with an input at 10 times the baud rate. The ones decade also provides the inputs for the ones distortion gate consisting of Z6, Z7, and Z8G1. When the number programmed by 1 PERCENT DISTORTION (outer) switch 1A1S2 is equal to the number in the ones decade, the output of the ones distortion gate is brought to ground (TP1). The tens distortion gate consisting of Z16, Z17, and Z18G4 are identical except the inputs are provided by the tens decade and controlled by the 10 PERCENT DISTORTION (inner) switch. The units and tens combiners are programmed for a specific number by the PERCENT DISTORTION switch. This number is equal to the amount and type of distortion selected by the PERCENT DISTORTION and DISTORTION SELECT switches. The unit distortion gates are inhibited through inverters Z9I1 and Z9I6 when the 1 PERCENT DISTORTION switch is at 0 and the DISTORTION SELECT switch is at M BIAS. The output of the tens decade provides inputs for clock output flip-flop Z12FF2. The detect 5 gate (Z15I1, 14, 15, and 16) detects a count of 5 and sets Z12FF2-Q to 0 at the end of the tens decade cycle, causing Z12FF2 to provide an output frequency at 2 times the baud rate.

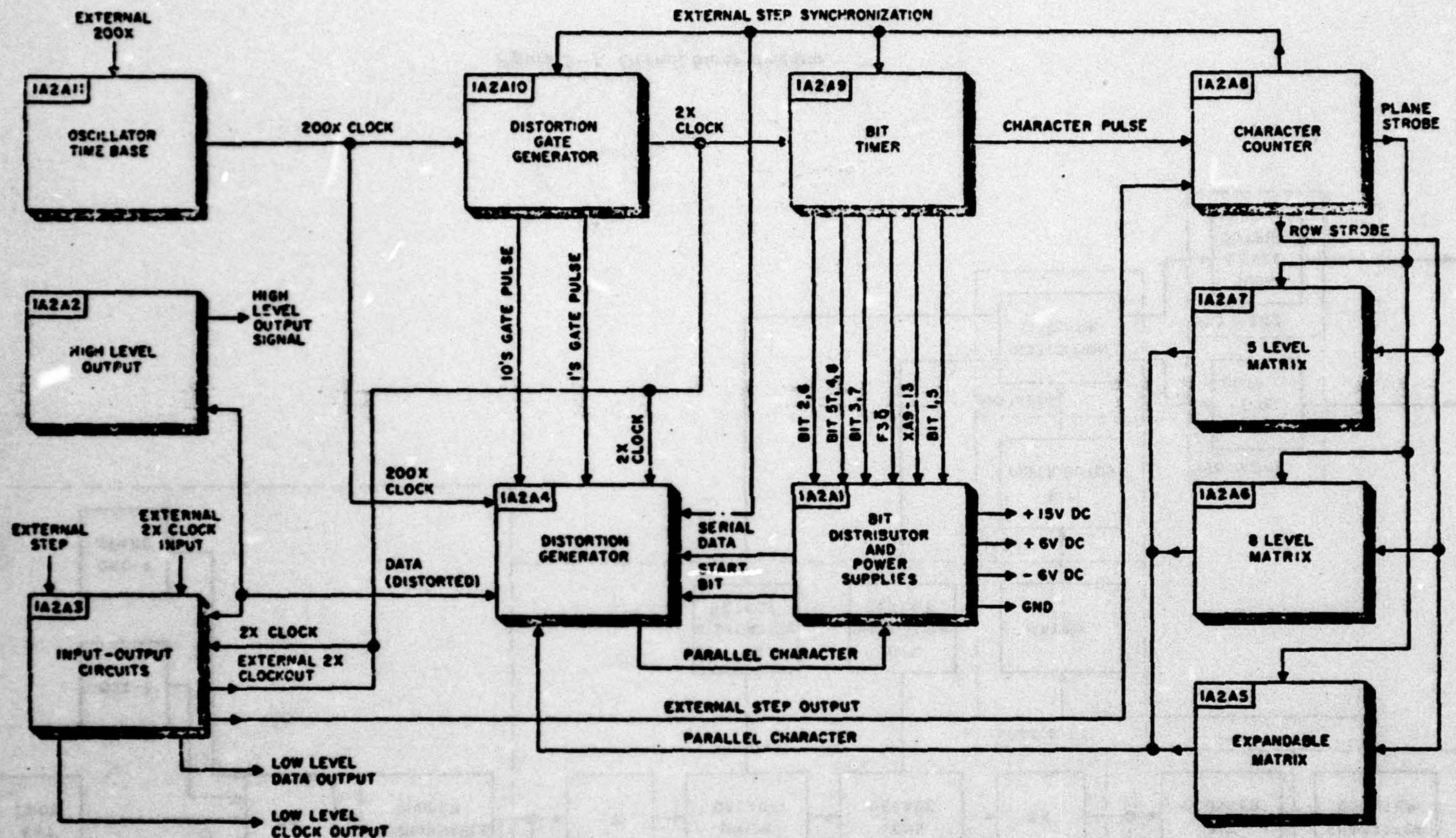

Figure 2—2. Simplified interconnection diagram.

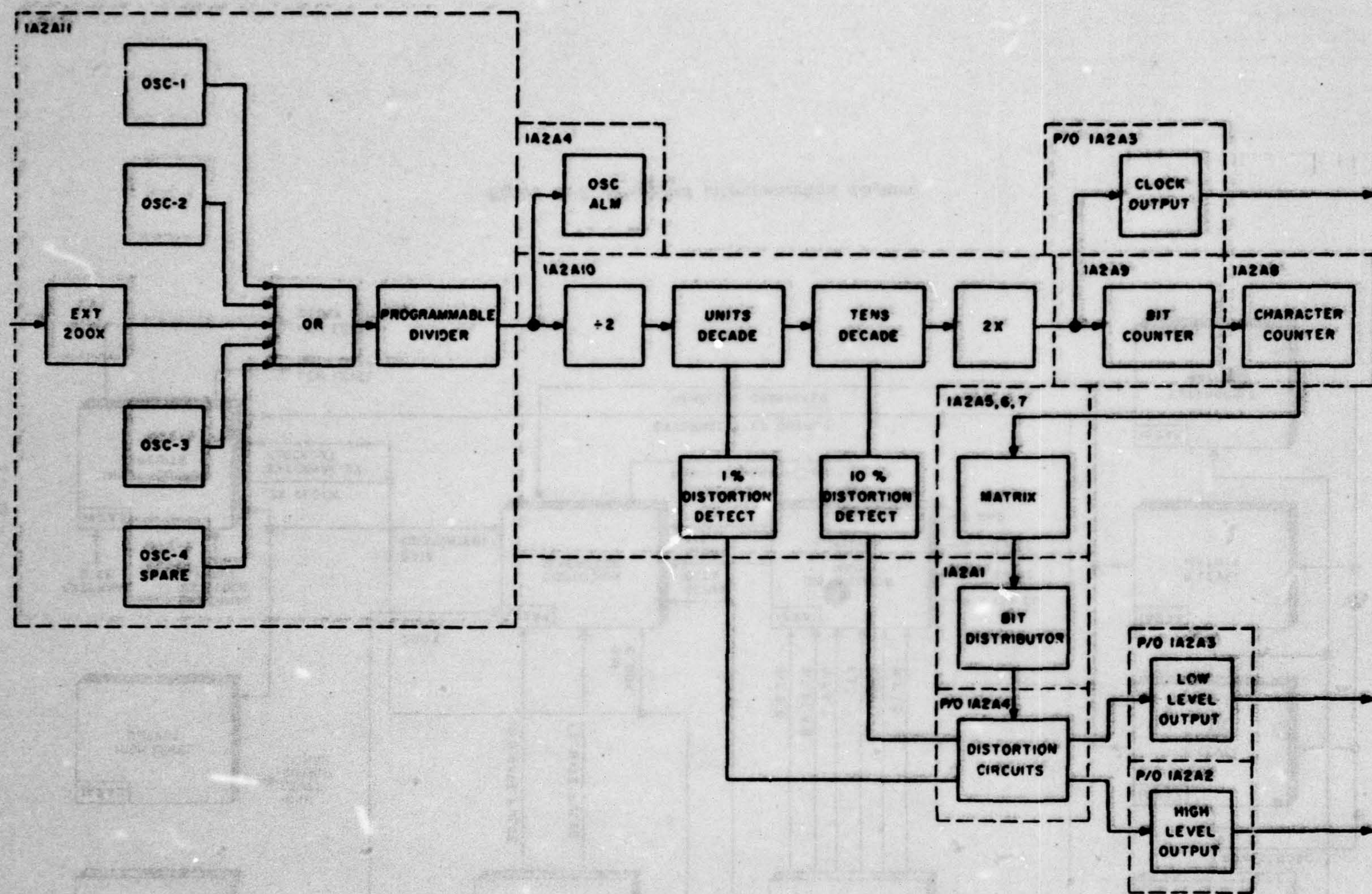

Figure 2—1. Overall block diagram.

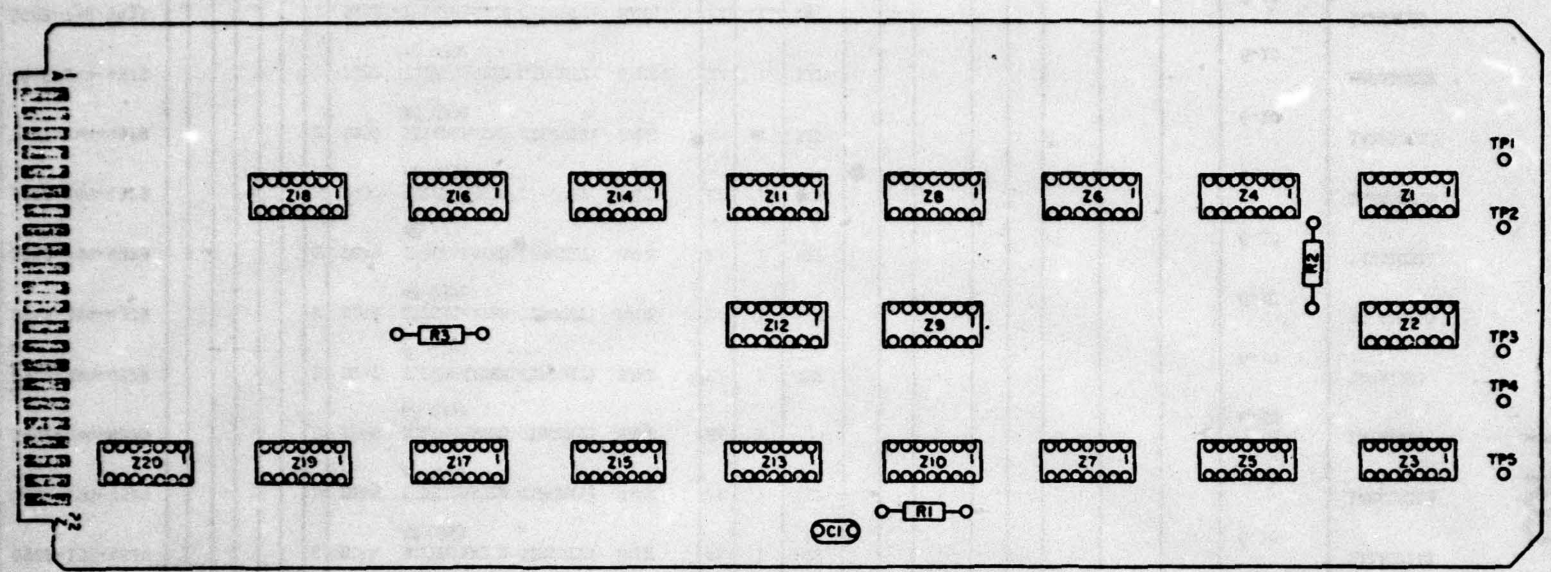

Figure 6—10. Assembly 1A2A10, component layout.

AND DEPOT MAINTENANCE

(2) FEDERAL STOCK NUMBER	MODEL 1	2	3	4	5	6	IND CD	(3) DESCRIPTION	UNIT OF ISSUE	QTY INC IN UN PK	QTY INC IN UNIT	30 DAY MAINT. ALW. DS (A) 1–20	DS (B) 21–50	DS (C) 51–100	GS (A) 1–20	GS (B) 21–50	GS (C) 51–100	1 YR. ALW. PER 100 EQUIP. CNTGCY PL.	DEPOT MAINT ALW. PER 100 EQUIP.	ILLUSTRATIONS (A) FIGURE NUMBER	(B) ITEM OR SYMBOL NUMBER
5925-441-9234							D	D139 COMPONENT BOARD ASSEMBLY: 14031; SMD633060	EA	1	1				2	2	2	71	3	6-10	1A2A10
5962-105-[illegible]							E	D140 CAPACITOR, FIXED, CERAMIC DIELECTRIC: 71590; CK502	EA	1	1								3	6-10	1A2A10C1
5962-105-4524							E	D141 INTERGRATED CIRCUIT: SAME AS C668	EA	1	REF									6-10	1A2A10Z1

C391 INTERGRATED CIRCUIT: 25677; U6A9946S9X

C422 RESISTOR, FIXED, COMPOSITION: 81349; RC20GF152J

C668 INTERGRATED CIRCUIT: 25677; U6A909359X

C395 INTERGRATED CIRCUIT: 25677; U6A9946S9X

C487 RESISTOR, FIXED, COMPOSITION: 81349; RC20GF562J

(2) FEDERAL STOCK NUMBER	MODEL 1	2	3	4	5	6	IND CD	(3) DESCRIPTION	UNIT OF ISSUE	QTY INC IN UN PK	QTY INC IN UNIT	DS 1–20	DS 21–50	DS 51–100	GS 1–20	GS 21–50	GS 51–100	1 YR. ALW.	DEPOT MAINT ALW.	FIGURE NUMBER	ITEM OR SYMBOL NUMBER
5962-105-4624							E	D142 INTERGRATED CIRCUIT: SAME AS C668	EA	1	REF									6-10	1A2A10Z2
5962-105-4624							E	D143 INTERGRATED CIRCUIT: SAME AS C668	EA	1	REF									6-10	1A2A10Z3
5962-105-4624							E	D144 INTERGRATED CIRCUIT: SAME AS C668	EA	1	REF									6-10	1A2A10Z12
5962-105-4624							E	D145 INTERGRATED CIRCUIT: SAME AS C668	EA	1	REF									6-10	1A2A10Z13
5962-344-4379							E	D146 INTERGRATED CIRCUIT: SAME AS C391	EA	1	7									6-10	1A2A10Z4
5962-344-4379							E	D147 INTERGRATED CIRCUIT: SAME AS C391	EA	1	REF									6-10	1A2A10Z5
5962-344-4379							E	D148 INTERGRATED CIRCUIT: SAME AS C391	F[illegible]	1	REF									6-10	1A2A10Z10
5962-344-4379							E	D149 INTERGRATED CIRCUIT: SAME AS C391	EA	1	REF									6-10	1A2A10Z11
5962-344-4379							E	D150 INTERGRATED CIRCUIT: SAME AS C391	EA	1	REF									6-10	1A2A10Z16
5962-344-4379							E	D151 INTERGRATED CIRCUIT: SAME AS C391	EA	1	REF									6-10	1A2A10Z18
5962-344-4379							E	D152 INTERGRATED CIRCUIT: SAME AS C391	EA	1	REF									6-10	1A2A10Z22
5962-739-3415							E	D153 INTERGRATED CIRCUIT: SAME AS C395	EA	1	8									6-10	1A2A10Z6

REPAIR PARTS FOR DIRECT SUPPORT, GENERAL SUPPORT, AND DEPOT MAINTENANCE

(2) FEDERAL STOCK NUMBER	MODEL 1	2	3	4	5	6	IND CD	(3) DESCRIPTION	(4) UNIT OF ISSUE	(5) QTY INC IN UN PK	(6) QTY INC IN UNIT	(7) 30 DAY MAINT. ALW. DS (A) 1-20	DS (B) 21-50	DS (C) 51-100	GS (A) 1-20	GS (B) 21-50	GS (C) 51-100	(8) 1 YR. ALW. PER 100 EQUIP. CNTGCY PL.	(9) DEPOT MAINT. ALW. PER 100 EQUIP.	(10) ILLUSTRATIONS (A) FIGURE NUMBER	(B) ITEM OR SYMBOL NUMBER
5962-789-3415							E	D154 INTERGRATED CIRCUIT: SAME AS C395	EA	1	REF									6-10	1A2A10Z7
5962-789-3415							E	D155 INTERGRATED CIRCUIT: SAME AS C395	EA	1	REF									6-10	1A2A10Z8
5962-789-3415							E	D156 INTERGRATED CIRCUIT: SAME AS C395	EA	1	REF									6-10	1A2A10Z14
5962-789-3415							E	D157 INTERGRATED CIRCUIT: SAME AS C395	EA	1	REF									6-10	1A2A10Z19
5962-789-3415							E	D158 INTERGRATED CIRCUIT: SAME AS C395	EA	1	REF									6-10	1A2A10Z20
5962-789-3415							E	D159 INTERGRATED CIRCUIT: SAME AS C395	EA	1	REF									6-10	1A2A10Z21
5962-789-3415							E	D160 INTERGRATED CIRCUIT: SAME AS C395	EA	1	REF									6-10	1A2A10Z23
							E	D161 PRINTED CIRCUIT BOARD: 14031; SMD632878	EA	1	1									6-10	1A2A10MP1
5905-195-6453							E	D162 RESISTOR, FIXED, COMPOSITION: SAME AS C487	EA	1	1									6-10	1A2A10R1
5905-279-1751							E	D163 RESISTOR, FIXED, COMPOSITION: SAME AS C422	EA	1	2									6-10	1A2A10R2
5905-279-1757							E	D164 RESISTOR, FIXED, COMPOSITION: SAME AS C422	EA	1	REF									6-10	1A2A10R3
							E	D165 STIFFENER, BAR: SAME AS C447	EA	1	REF									6-10	1A2A10MP2

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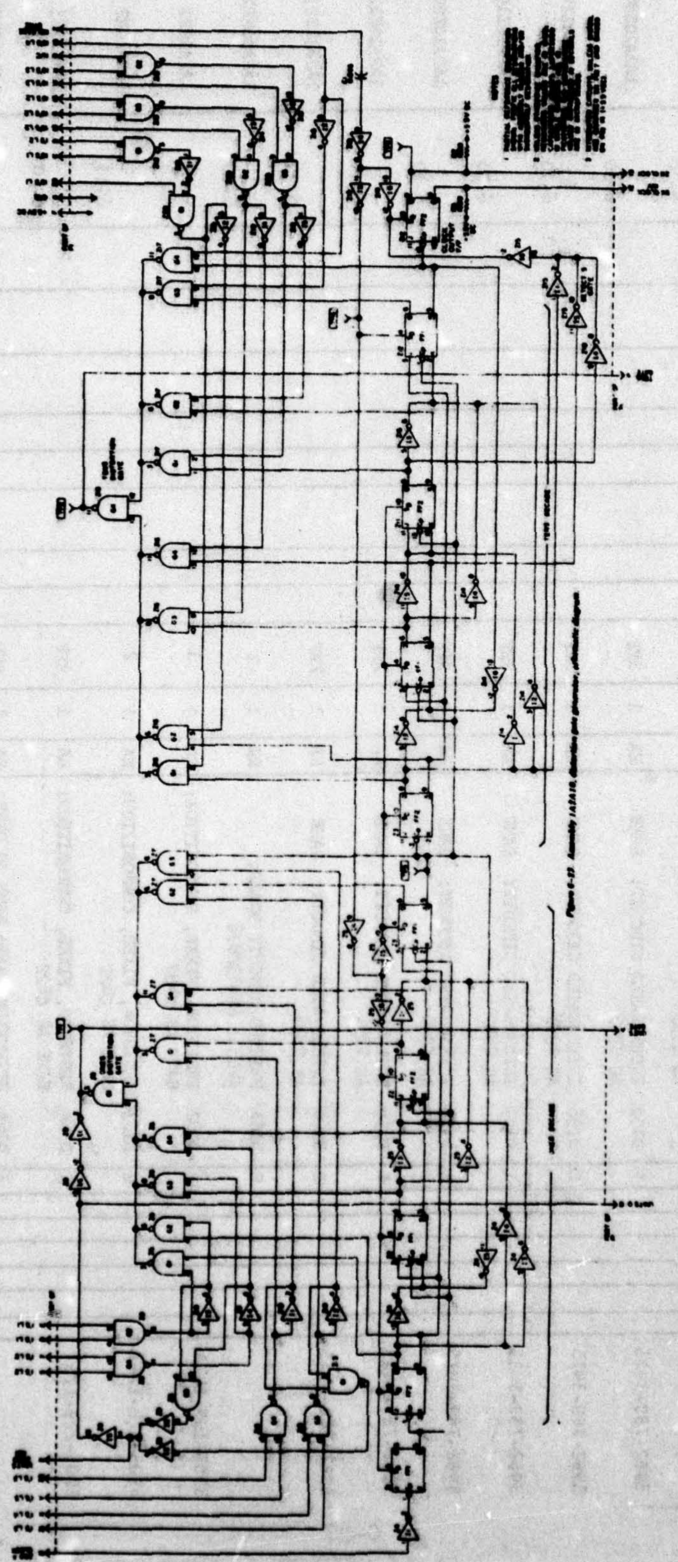

APPENDIX B

ISLS PULSE TIMER SINGLE-SHOTS
(FIGURE FO-72)

a. The ISLS pulse timer on mode 4 and mode 4 test challenge video card A25 employs two single-shots to produce properly timed ISLS pulses as discussed in Paragraph 5-19. One of these is single-shot U6, which is an integrated circuit adequately described in Chapter 2. However, the other single-shot, composed of AND U13A, OR's U8B and U15A, inverter U11A, and capacitor C3, requires further explanation.

b. After each ISLS pulse (fifth bit + P2), and until 2 microseconds before the next ISLS pulse, single-shot U6 is in its quiescent state, delivering a high $\overline{Y}$ output to AND U13A and OR U8B. However, the output of AND U13A is high, because its other input from OR U8B is low, or is rapidly going low. (With two high inputs, the output of AND U13A would be low, forcing a high output from OR U15A after the brief interval required to charge C3; but a high output from OR U15A, together with the high $\overline{Y}$ output of U6, causes OR U8B to deliver a low output to AND U13A.) Thus, after U6 has been in its quiescent state for 0.2 microsecond or longer, the output of AND U13A is high and the output of inverter U11A is low, corresponding to the complementary "$\overline{Y}$" and "Y" outputs of a single-shot in its quiescent state.

c. When single-shot U6 is triggered by an $(\text{SIF P1})^{-1}$, its $\overline{Y}$ output goes low for the adjustable duration of the ISLS pulse delay (nominally 2 microseconds). This forces a high output from OR U8B to AND U13A, but the low $\overline{Y}$ output of U6 now maintains the high output from AND U13A. With two high inputs, OR U15A quickly discharges C3 as its output goes low. Thus, the low $\overline{Y}$ output of U6 changes the "state" of OR's U8B and U15A, but does not change the high "$\overline{Y}$" output of AND U13A or the low "Y" output of inverter U11A.

d. At the end of the ISLS pulse delay, when the $\overline{Y}$ output of U6 goes high, AND U13A momentarily has two high inputs, and its output goes low and causes the output of inverter U11A to go high. These levels correspond to the low $\overline{Y}$ and high Y outputs of a single-shot that has been triggered into its active state. The low output from AND U13A immediately causes OR U15A to start charging C3 for a high output that will restore the quiescent condition described in b. above. The value of C3 causes a delay of approximately 0.2 microseconds before the quiescent condition is reached, and the complementary $(\text{fifth bit + P2})^{-1}$ and fifth bit + P2 outputs from AND U13A and inverter U11A therefore have a pulse width of approximately 0.2 microsecond.

MODE 1 AND TEST CHALLENGE
VIDEO ASSY

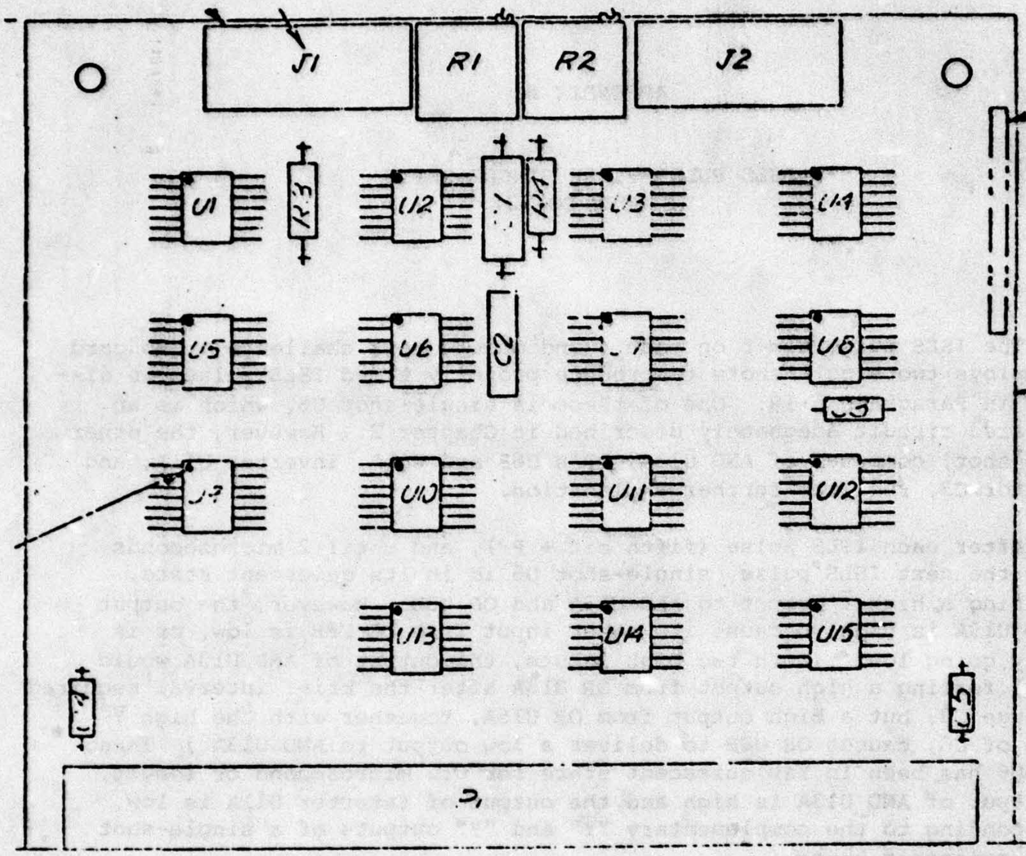

TABLE OF ELECTRICAL PARTS	
REF DES	FIND NO.
C1	17
C2	11
C3	16
C4, C5	15
J1, J2	10
P1	19
R1, R2	20
R3, R4	18
U1	8
U2, U6	9
U3, U9	4
U4	6
U5	7
U7	3
U8, U13, U14, U15	1
U10, U12	5
U11	2

ASSEMBLY

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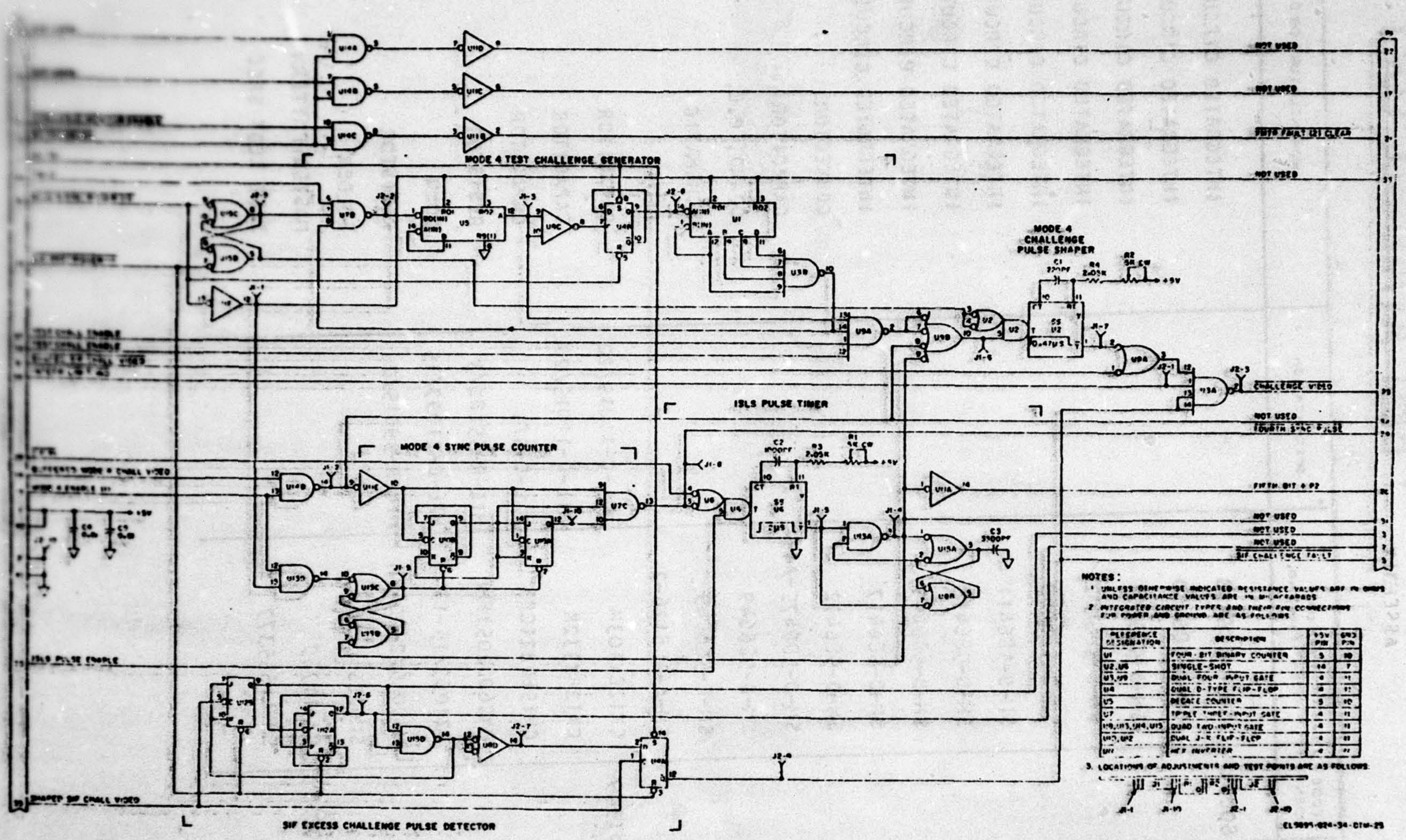
FIND NO.	QTY REQ'D	CODE IDENT	PART OR IDENTIFYING NO.	SPECIFICATION	NOMENCLATURE OR DESCRIPTION
1	4	80063	SM-B-586398		INTEGRATED CIRCUIT
2	1		SM-B-586400		INTEGRATED CIRCUIT
3	1		SM-B-586401		INTEGRATED CIRCUIT
4	2		SM-B-586402		INTEGRATED CIRCUIT
5	2		SM-B-586409		INTEGRATED CIRCUIT
6	1		SM-B-586411		INTEGRATED CIRCUIT
7	1		SM-B-586413		INTEGRATED CIRCUIT
8	1		SM-B-586415		INTEGRATED CIRCUIT
9	2		SM-B-586417		INTEGRATED CIRCUIT
10	2		SM-D-586472		CONNECTOR
11	1		SM-D-586475-A13		CAPACITOR
12	1		SM-D-586649		BOARD, P.C.
13	REF		SM-E-586849		SCHEMATIC
14	AR		SM-A-588136-2		FLUX
15	2	81349	CK12BX103M	MIL-C-11015/20	CAPACITOR
16	1		CK12BX332K	MIL-C-11015/20	CAPACITOR
17	1		CM15ED221GP3	MIL-C-5/1	CAPACITOR
18	2		RNC60J2051FM	MIL-R-55182/3	RESISTOR
19	1		M21097/15-13	MIL-C-21097/15	CONN
20	2		M39015/2-006PM	MIL-R-39015/2	RESISTOR
21	AR		SN60BS		SOLDER
22	REF	80063	MP-11769		MASTER PATTERN
23	REF		SM-A-635377		TEST REQT SPEC



FO-72. Mode 4 test challenge video card A25, schematic diagram.

APPENDIX C

MODULAR CARRIER GENERATOR CIRCUIT CARD ASSEMBLY 10281636

The following paragraphs describe the card components and their functional operation.

a. General Description. The modulator carrier generator circuit card contains 30 integrated circuit logic devices. The schematic diagram for circuit card 10281636 is provided on FO-19. The logic devices contain the following logic components: five 4-bit binary counters (U27 through U31), ten two-input NAND gates (U1, U2, U4, U8, U9, U14 through U17, and U26), two three-input NAND gates (U7 and U32), three four-input NAND gates with expander inputs (U10, U11, and U12) and five dual J-K flip-flops (U12, U13, U20, and U23). The logic devices are connected to perform frequency shift-keying (FSK) and differential frequency shift-keying (DFSK) modulation, when used in conjunction with external modem cards.

b. Circuit Description. The modulator carrier generator circuit card converts bit-rate control and frequency control (modulation) information into 4-bit, binary-weighted signals representing the FSK/DFSK carrier. The card logic performing this operation consists of three functional sections: an up-down counter, a variable divider, and a transmit clock generator. A description of each functional section is provided as follows:

(1) Variable divider. The variable divider interprets bit-rate and frequency-control input data to produce a variable division factor (÷18 to ÷44) that ultimately controls the frequency of the output carrier. The divider circuit (upper half of FO-19) consists of a bit-rate selector, a variable counter, and a fraction counter. The bit-rate selector logic decodes 7-bit binary input data representing frequency control (F_m, F_C, F_S) and bit-rate select (600 BPS, 1200 BPS, 750 BPS, 1500 BPS)$^{-1}$ information. The decoded data is applied to parallel data inputs A through D of 4-bit binary counters U27 and U28, with the A input to U27 being the least significant bit (2^0), and the D input to U28 being the most significant bit (2^7). Inputs C and D to U28 are both tied to 5 Vdc; therefore, bit positions 2^6 and 2^7 are always in a logical ONE state. The combined counters comprise a 256-bit variable counter that performs the actual division. The parallel input data presets the counter to an initial count that determines the division factor. The counter is then permitted to serially count 1.584 MHz clock pulses until the maximum value is reached. The difference between the preset value and the maximum value is the divisor.

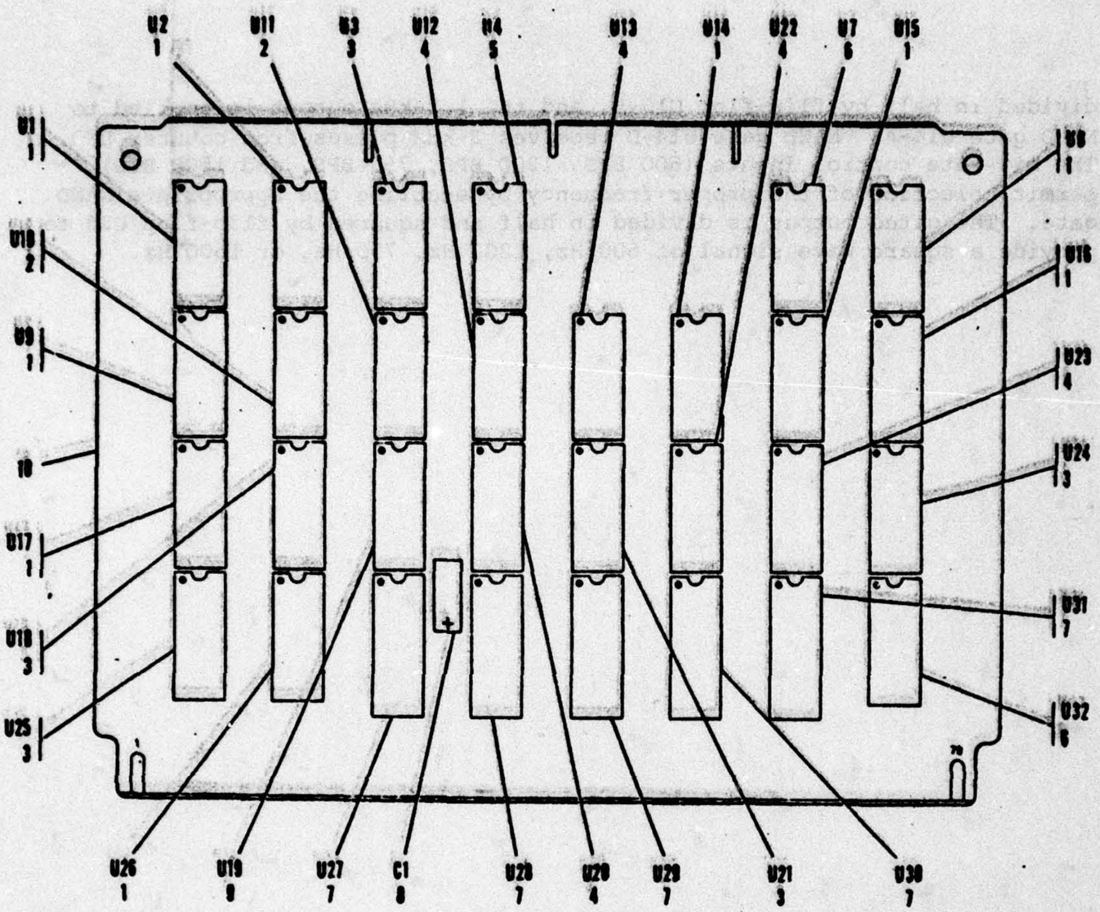
For example, assume that the counter is preset to decimal 218, or binary 0 1 0 1 1 0 1 1. Because the maximum value is 256, the counter will count 38 clock pulses before producing a high level at the C_0 output of U28 (256 - 218 = 38). When the input clock pulse again goes positive, pin 8 of NAND gate U4 goes low, enabling the $LOAD^{-1}$ inputs to U27 and U28. This again presets the counter to 218 and it counts 38 additional clock pulses before producing another output pulse. A fraction counter, consisting of four J-K flip-flops (U12 and U20) and associated logic, is used in conjunction with the variable counter when the divisor required to produce the desired carrier is not a whole integer. The fraction counter is essentially a divide-by-eight shift counter that provides feedback to the preset inputs of the variable counter through the input-control circuitry. As an example of circuit operation, assume that a divisor of 29-1/8 is required to produce the correct carrier frequency. The variable counter is initially preset to perform a divide-by-29 operation. The fraction counter allows the variable counter to divide by 29 seven times, then forces it to perform a divide-by-30 operation on the eighth time. The average division factor for each operation is then 29-1/8.

(2) Up-down counter. The up-down counter converts variable-frequency clock pulses from the variable counter into 4-bit binary-coded outputs representing the carrier frequency. The up-down counter consists of 4-bit binary counter U31, J-K flip-flop U23, and associated gating logic. The circuit is essentially a divide-by-32 up counter that initiates a down count every 16 clock times by gating the complement of the up count. The resulting 4-bit binary outputs produced during the first 16 clock times are complementary to the binary outputs produced during the second 16 clock times. The clock pulses are serially counted by 4-bit binary counter U31. J-K flip-flop U23 determines whether the count is up or down by enabling the proper gating circuits. After counting 16 clock pulses, the C_0 output of U31 goes low, causing U23 to switch to the opposite state. This gates the complement of the previous count for the next 16 clock pulses. The resulting 4-bit binary code is eventually transformed to a carrier frequency after digital-to-analog conversion is performed.

(3) Transmit clock generator. The transmit clock generator converts bit-rate input data into a variable division factor and produces square-wave signals at selected frequencies of 600 Hz, 1200 Hz, 750 Hz, and 1500 Hz. The square-wave generating circuitry consists of divide-by-16 counter U30, divide-by-10 counter U29, and divide-by-2 flip-flops U13-A, U-13-B, U22, and U23. Selection of the proper bit rate is controlled through NAND gates U14-A through U14-D. Four-bit binary counters U29 and U30 provide primary frequency division by dividing the 48-kHz input clock pulses by factors of 10 and 16, respectively. Counter U30 produces one output pulse for every 16 clock pulses received (3 kHz). Counter U29 produces one pulse for every 10 pulses received (4.8 kHz) because this counter is preset to an initial value of six at the start of each count. The resulting 4.8 kHz and 3-kHz pulse rates are again divided by two through J-K flip-flops U22 and U13-A, and the 1.5-kHz and 2.4-kHz square-wave outputs are applied to NAND gates U14-C and U14-B. In addition, the 2.4-kHz output from flip-flop U13-A is

divided in half by flip-flop U13-B, and the 1.2-kHz output is applied to NAND gate U14-A. NAND gate U14-D receives 3-kHz pulses from counter U30. The bit-rate control inputs (600 BPS, 1200 BPS, 750 BPS, and 1500 BPS)$^{-1}$ permit selection of the proper frequency by enabling the appropriate NAND gate. The gated output is divided in half and squared by flip-flop U23 to provide a square wave signal of 600 Hz, 1200 Hz, 750 Hz, or 1500 Hz.

Generator Carrier Modulation Circuit Card Assembly



REPAIR PARTS LIST

(1) ILLUSTRATION (A) FIG. NO.	(B) ITEM NO.	(2) SMR CODE	(3) NATIONAL STOCK NUMBER	(4) PART NUMBER	(5) FSCM	(6) DESCRIPTION USABLE ON CODE	(7) UNIT OF MEAS	(8) QTY INC IN UNIT
						GENERATOR CARRIER MODULATOR CIRCUIT CARD ASSY 10281636		
17-	1	PAHZZ		M1S19501-69	18876	MICROCIRCUIT	EA	9
17-	2	PAHZZ		M1S19501-59	18876	MICROCIRCUIT	EA	2
17-	3	PAHZZ		M1S19501-78	18876	MICROCIRCUIT	EA	5
17-	4	PAHZZ		862200-16	13973	MICROCIRCUIT	EA	5
17-	5	PAHZZ		M1S19561-37	18876	MICROCIRCUIT	EA	1
17-	6	PAHZZ	5962010206859	862209-16	13973	MICROCIRCUIT	EA	2
17-	7	PAHZZ		M1S19501-62	18876	MICROCIRCUIT	EA	5
17-	8	PAHZZ	5910009324435	M39003-01-2289	81349	CAPACITOR, FIXED, ELECTROLYTIC	EA	1
17-	9	PAHZZ		M1S19501-93	18876	MICROCIRCUIT	EA	1
17-	10	XAHZZ		10288117	18876	PRINTED WIRING BOARD	EA	1

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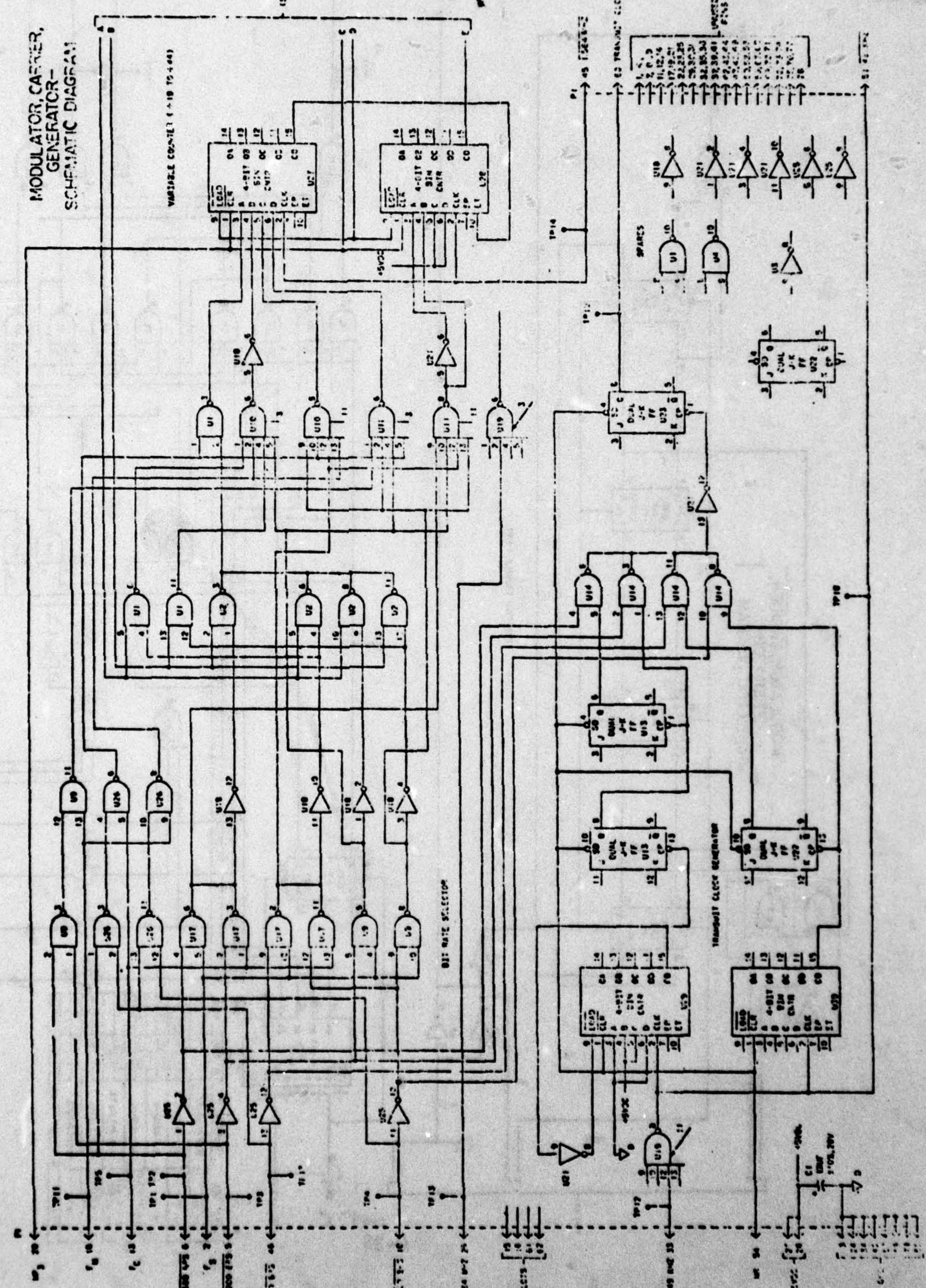

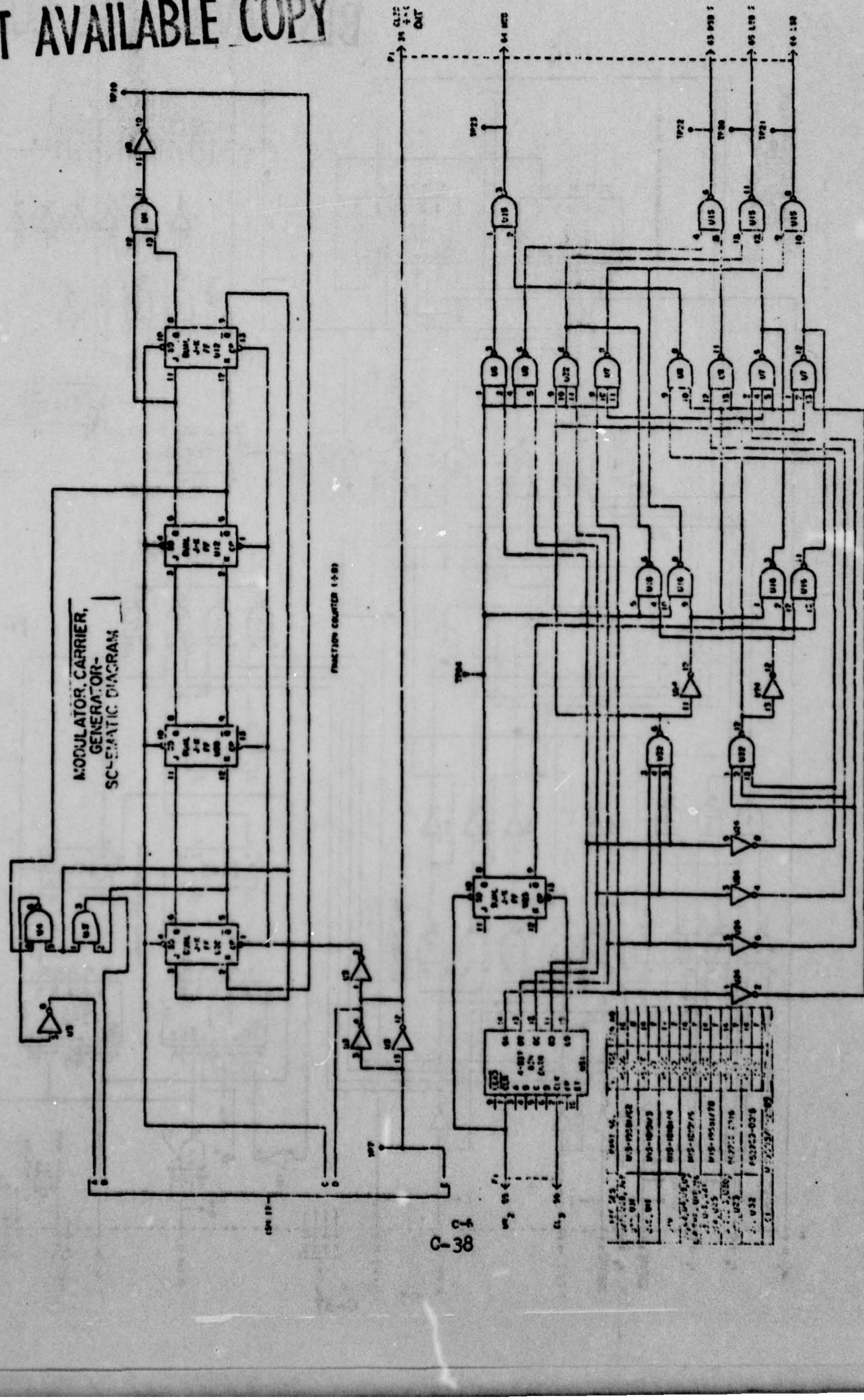
MODULATOR, CARRIER, GENERATOR- SCHEMATIC DIAGRAM

APPENDIX D

RF SWITCH DRIVER CARD A32A2
(FIGURE FO-81)

The RF switch driver card supplies the turn-on and turn-off voltages for the four switching diodes in the RF switch. The RF switch driver card also contains three check comparators which monitor RF switch operation. Turn-on check comparator Q9 checks that (RF switch drive)$^{-1}$ is positive enough to forward-bias the four diodes in the RF switch. The output of Q8 is applied to turn on check comparator Q9 through diode CR9 and resistor R21. When Q8 is turned off (which is true for all times except during a 0.6 microsecond period after the end of the ISLS gate), the input of Q9 is clamped to ground through diode CR8 and a high (turn-on test)$^{-1}$ signal is applied to the RF switch fault accumulator. At the end of the ISLS gate, Q8 is turned on to apply a high positive voltage to the base of Q9. This high level causes comparator Q9 to turn on and drop the (turn-on test)$^{-1}$ signal to near zero. At the end of the 0.6 microsecond period the output from Q8 returns to a low and the output of Q9 returns to a high. Short circuit check comparator Q11 checks for short circuits in any of the switching diodes in the RF switch. During ISLS gate time the output of turn-off driver Q5 drops to nearly -68 volts dc and draws the (RF switch drive)$^{-1}$ signal down to very near the same voltage. This negative voltage is applied to the base of Q11 through diode CR11 and resistor R25. Q11 is turned on and a high short circuit test signal is applied to the RF switch fault accumulator. A shorted diode prevents the negative swing of the (RF switch drive)$^{-1}$ signal; in this case, Q11 remains turned off and a low short circuit test signal (indicating a fault) results. Open circuit check comparator Q7 checks for open circuits in the four diodes of the RF switch. Between ISLS gates the (driver output)$^{-1}$ signal is clamped to approximately 0.7 volts (the voltage across one of the diodes) and draws the (RF switch drive)$^{-1}$ signal to very near the same voltage. This low voltage is applied to the base of Q7 through diode CR7 and resistor R16. Q7 is turned off and held off by a ground applied through diode CR5. As a result a high (RF sw open circuit fault)$^{-1}$ is applied to the RF switch fault accumulator. An open-circuited diode prevents the driver output signal [and similarly the (RF switch drive)$^{-1}$ signal] from being clamped to 0.7 volts; the signal level increases to +12 volts. This +12 volt level causes Q7 to turn on and drop the (RF sw open circuit fault)$^{-1}$ signal to near zero, indicating a fault.

SWITCH DRIVER ASSY

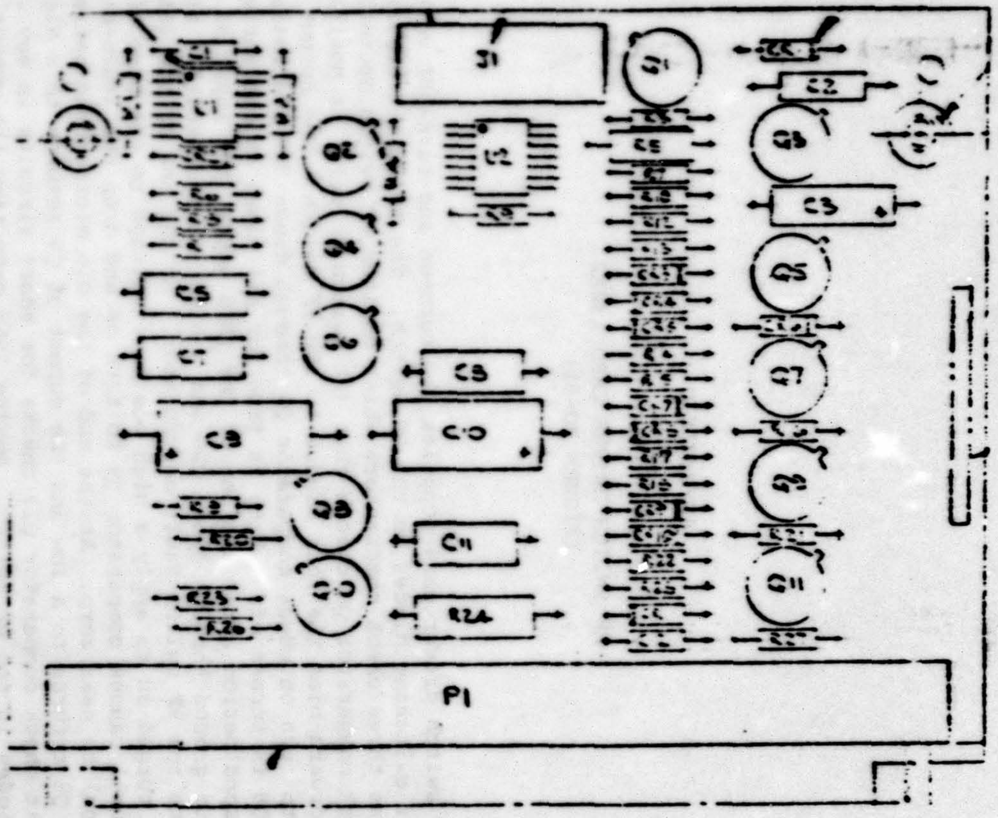

TABLE OF ELECTRICAL PARTS		
REF. DES		FIND NO.
R1, R4 R6 R9 R18 R26		22
R2		30
R3, R20 R26		21
R5		34
R7, R12		28
R8 R... R27		25
R10 R13 R18 R23		27
R14		23
R16 R17		29
R22, R21		24
R24		35
R25		26
C1		31
C2 C5 C7 C8, C11		33
C3		36
—		—
C9		37
C10		40
C12		32
J1		5
P1		38
U1		2
U2		11
Q1 Q8 Q10		3 & 4
Q2		7 & 3
Q3		20 & 4
Q4, Q6		9 & 4
Q5		8 & 4
Q7 Q9		6 & 3
Q11		9 & 3
CR1	▲	15
CR2, 3 4 5 8 10	▲	13
CR6 7 9. 11	▲	12

REF DES	PART NO.	VOLTAGE	PIN NO.
U1 THRU U12	MIS19581/76	+5V (P)	4
		[illegible]	8
C1, C2	M39014/05-[illegible]		
K1	[illegible]		
VR1 THRU VR3	JAN1N[illegible]		

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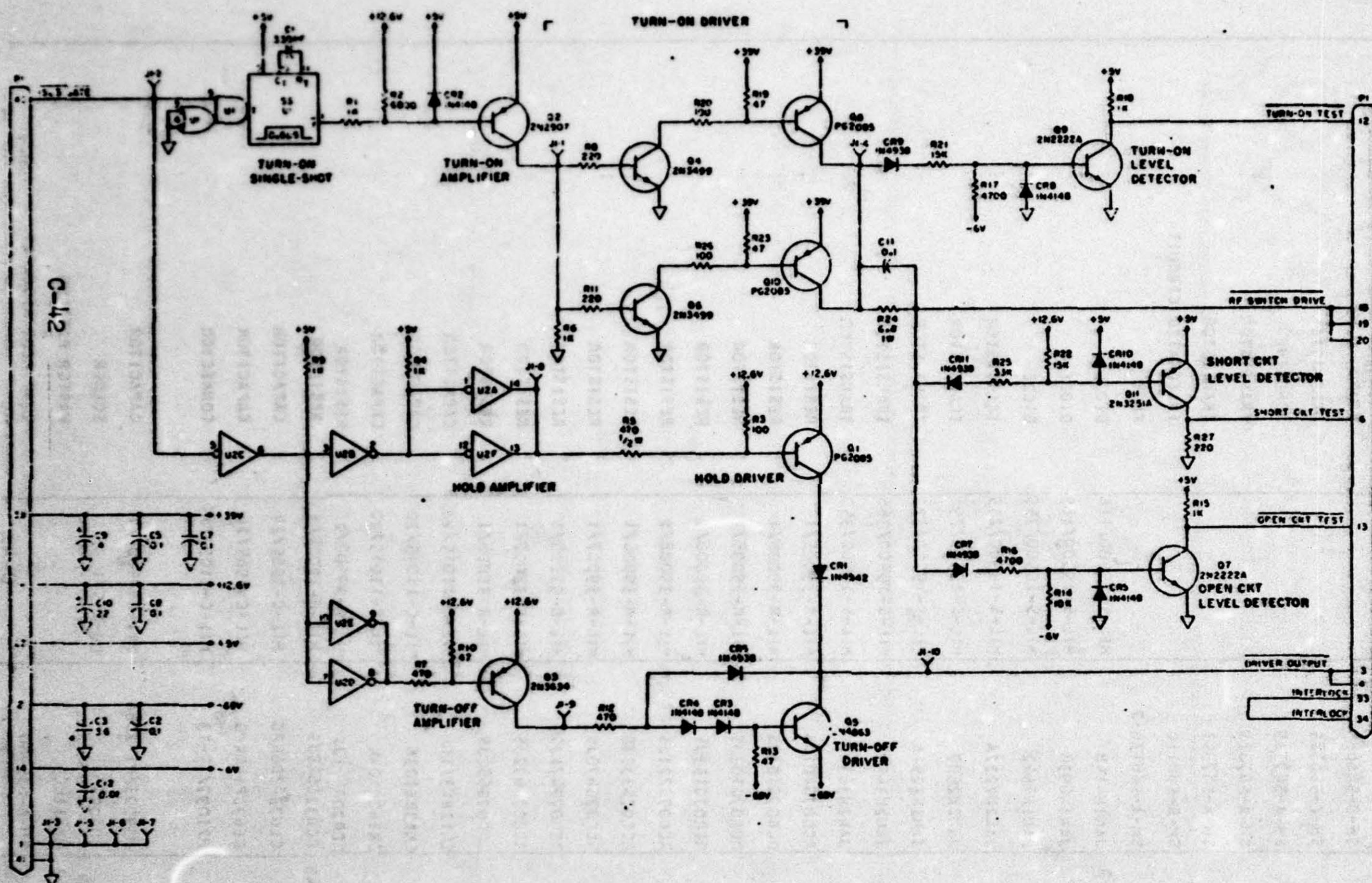
PARTS LIST FOR
SWITCH DRIVER ASSEMBLY

FIND NO.	QTY REQ'D	CODE IDENT	PART OR IDENTIFYING NO.	SPECIFICATION	NOMENCLATURE OR DESCRIPTION	NOTES
1	2	80063	SM-A-586327-7/6		INSERT, SCREW THREAD	
2	1		SM-B-586417		INTEGRATED CIRCUIT	
3	4		SM-B-586452		TRANSISTOR PAD	
4	7		SM-A-586460		TRANSISTOR PAD	
5	1		SM-D-586472		CONNECTOR	
6	1		SM-D-586685		BOARD, P.W.	
7	REF		SM-E-586885		SCHEMATIC	
8	AR		SM-A-587719		ADHESIVE	
9	1		SM-A-587919		TRANSISTOR	
10	3		SM-A-587953		TRANSISTOR	
11	1		SM-B-588110		INTEGRATED CIRCUIT	
12	AR		SM-A-588136-2		FLUX	
13	6	81349	JAN1N4148	MIL-S-19500/116	DIODE	
14	4		JAN1N4938	MIL-S-19500/169	DIODE	
15	1		JAN1N4942	MIL-S-19500/359	DIODE	
16	2		JAN2N2222A	MIL-S-19500/255	TRANSISTOR	
17	1		JAN2N2907	MIL-S-19500/291	TRANSISTOR	
18	1		JAN2N3251A	MIL-S-19500/323	TRANSISTOR	
19	2		JAN2N3499	MIL-S-19500/366	TRANSISTOR	
20	1		JAN2N3634	MIL-S-19500/357	TRANSISTOR	
21	3		RCR07G101JS	MIL-R-39008/1	RESISTOR	
22	6		RCR07G102JS	MIL-R-39008/1	RESISTOR	
23	1		RCR07G103JS	MIL-R-39008/1	RESISTOR	
24	2		RCR07G153JS	MIL-R-39008/1	RESISTOR	
25	3		RCR07G221JS	MIL-R-39008/1	RESISTOR	
26	1		RCR07G333JS	MIL-R-39008/1	RESISTOR	
27	4		RCR07G470JS	MIL-R-39008/1	RESISTOR	
28	2		RCR07G471JS	MIL-R-39008/1	RESISTOR	
29	2		RCR07G472JS	MIL-R-39008/1	RESISTOR	
30	1		RCR07G682JS	MIL-R-39008/1	RESISTOR	
31	1		CK12BX331K	MIL-C-11015/20	CAPACITOR	
32	1		CK13BX103K	MIL-C-11015/20	CAPACITOR	
33	5		CK14BR104K	MIL-C-11015/20	CAPACITOR	
34	1		RCR20G471JS	MIL-R-39008/2	RESISTOR	
35	1	81349	RCR32G683JS	MIL-R-39008/3	RESISTOR	
36	1		CL67BP3R6KPG	MIL-C-3965/24	CAPACITOR	
37	1		CL67BP140KPG	MIL-C-3965/24	CAPACITOR	
38	1		M21097/15-13	MIL-C-21097/15	CONNECTOR	
39	-					
40	1		M39003/01-2066	MIL-C-39003/1	CAPACITOR	
41	AR		SN60BS	QQ-S-571	SOLDER	
42	REF	80063	MP-11805		MASTER PATTERN	
43	REF		SM-A-635400		TEST REQT ASSEMBLY	D-3

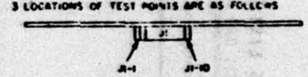


NOTES:

1. UNLESS OTHERWISE INDICATED RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.
2. INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS.

REFERENCE DESIGNATION	DESCRIPTION	+5V PIN	GND PIN
U1	SINGLE-SHOT	14	7
U2	HEX INVERTER (OPEN COLLECTOR)	4	11

3. LOCATIONS OF TEST POINTS ARE AS FOLLOWS



FO-81. RF switch driver card A32A2, schematic diagram.

APPENDIX E

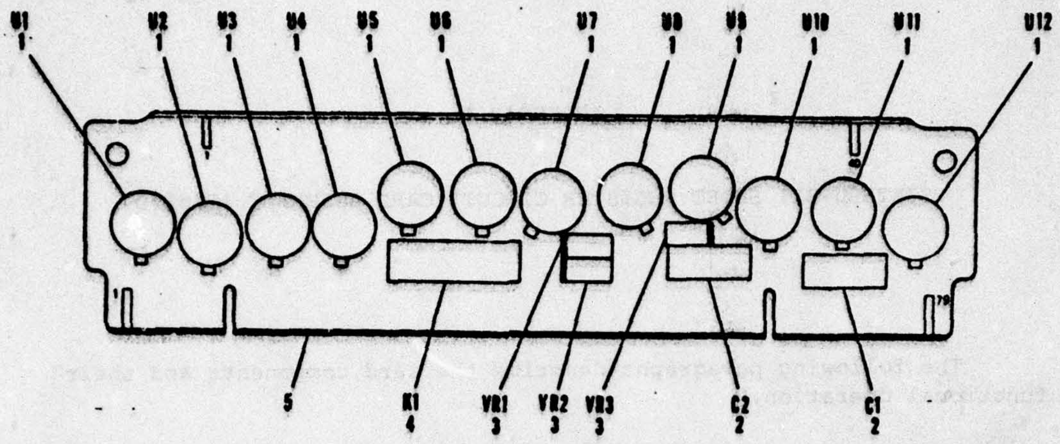
SIXTEEN-BIT SHIFT REGISTER CIRCUIT CARD ASSEMBLY 10281707

The following paragraphs describe the card components and their functional operation.

a. General Description. The 16-bit shift register circuit card contains 12 integrated circuit logic devices. Each device contains two 16-bit shift registers for a total of 24 shift registers. The schematic diagram for the 10281707 card is provided on FO-22.

b. Circuit Description. The 16-bit shift register circuit card is enabled during normal operation when 5 Vdc and 15 Vdc are applied to respective card inputs. The 5 Vdc energizes relay K1 to distribute 5 Vdc to the logic components through the energized relay contacts. During in-shelter card testing with the MTS, relay K1 is deenergized and 5 Vdc is supplied from the MTS test probe through test point TP8A. The logic components also require 12 Vdc. The available 15 Vdc is decreased by approximately 3 Vdc through voltage regulators diodes VR1, VR2, and VR3, and the three 12 Vdc outputs are applied to groups of logic components as shown on FO-22. The 16-bit shift registers (U1 through U12) then respond to their respective inputs in accordance with the truth table. Each 16-bit shift register receives serially applied data (DATA A and DATA B) in synchronization with clock pulses applied through the common CLOCK line. The first data bit entered is shifted 1-bit position through the register for each transition of the clock pulse. Therefore, after 16 clock pulses have occurred, the respective output (DOA or DOB) will assume the logic state of the data bit initially entered. Thus, the input data is effectively delayed by the period of the clock pulse multiplied by 16. Each additional data bit entered is processed in the same manner.

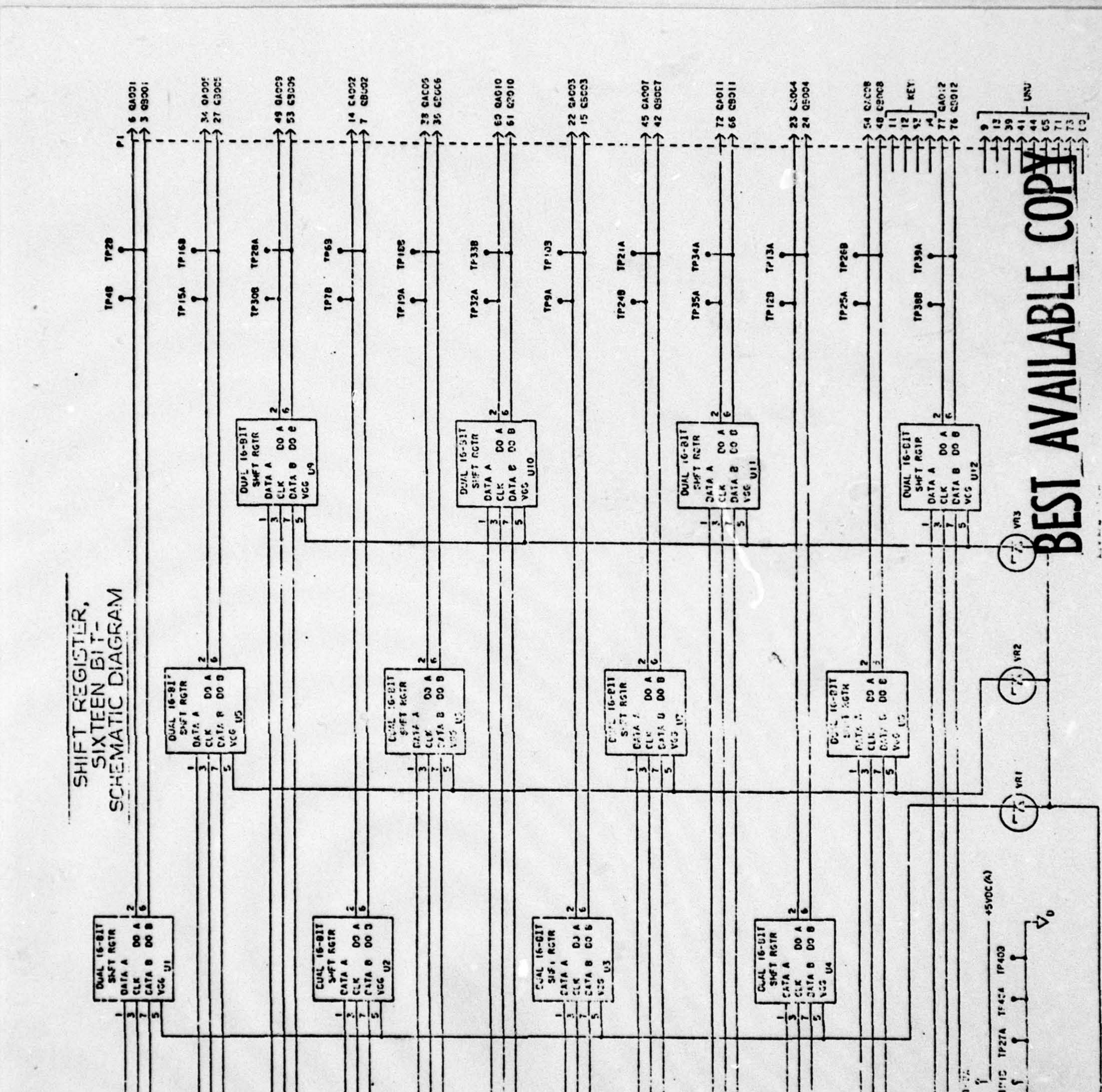
16-Bit Shift Register Circuit Card Assembly



REPAIR PARTS LIST

(1) ILLUSTRATION (A) FIG. NO.	(B) ITEM NO.	(2) SMR CODE	(3) NATIONAL STOCK NUMBER	(4) PART NUMBER	(5) FSCM	(6) DESCRIPTION USABLE ON CODE	(7) UNIT OF MEAS	(8) QTY INC IN UNIT
						16 BIT SHIFT REGISTER CIRCUIT ASSY 10281707		
20-	1	PAHZZ		M1819581-76	18876	MICROCIRCUIT	EA	12
20-	2	PAHZZ		M39014-05-0498	81349	CAPACITOR, FIXED, CERAMIC	EA	2
20-	3	PAHZZ	5961009475714	1N4371A	81349	SEMICONDUCTOR DEVICE, DIODE	EA	3
20-	4	PAHZZ		10282561	18876	RELAY, ARMATURE	EA	1
20-	5	XAHZZ		10283543	18876	PRINTED WIRING BOARD	EA	1

SHIFT REGISTER, SIXTEEN BIT-SCHEMATIC DIAGRAM



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AD-A050 269 ARINC RESEARCH CORP ANNAPOLIS MD F/G 14/2

DETERMINATION OF THE BEST SET OF CHARACTERISTICS FOR AN US ARMY--ETC(U)

DEC 77 L GRAHAM, A SIMMONS DAEA18-72-A-0005

UNCLASSIFIED 1073-0420-1662 ECOM-72-0005-F NL

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ARINC

A Subsidiary of Aeronautical Radio, Inc

2551 Riva Road • Annapolis, Maryland 21401

July 14, 1977
DC^{3}G/TSP-77-141
Contract DAEA 18-72-A-0005
Work Order 1073-04

Attention:

Subject: Digital Card Tester (DCT) Program Users' Survey

Dear Sir:

ARINC Research Corporation, a consulting and engineering research company, was recently awarded a six-month contract (DAEA 18-72-A-0005) to assist the U.S. Army Electronics Command (ECOM) in determining the best set of characteristics for a general purpose semi-automatic Digital Card Tester (DCT) that meets U.S. Army testing requirements. The program is being planned and administered by the TMDE Division of the Directorate of Maintenance of Ft. Monmouth, New Jersey.

The ARINC Research project in support of this program consists of several tasks, starting with an evaluation of the Semi-Automatic General Purpose Digital Card Tester market and ending with the identification of parameters for a DCT. The initial effort was directed at a review of the technological trends of the DCT industry and the selection of up to 20 DCTs for further analysis.

The next two tasks in the DCT project consist of two surveys; one directed at the DCT manufacturers and the second directed at current and potential DCT users within the U.S. Army. The purpose of the manufacturers' survey is to determine the best DCT test methodology and set of characteristics available on the commercial market. The users' survey is required in order to catalog the intended maintenance role(s) of the DCT in the Army. The users' survey also seeks data on material requirements, training, and employment limitations that will provide ECOM with a more comprehensive understanding of the scope and need for a DCT.

Phones: Annapolis 301-224-4000 | Washington, D. C. 261-8100 | Santa Ana, Calif. 714-547-7584 | TWX: Annapolis 710-867-8663 | Santa Ana, Calif. 910-595-1110

Your organization has been recommended by the Contracting Officer's Representative as a potential source of data for the users' survey; under his direction, this letter and the enclosed survey form are forwarded to your office for action. In addition to requesting data, the survey document provides information on the DCT program. Your comments and questions concerning the DCT program or specific requested data elements should be directed to the COR or the ARINC Research Corporation points of contact as indicated in the survey.

Because of the time constraints of the contract, your response to the survey questions must be received by ARINC Research Corporation no later than 19 August 1977. Responses received after that date may not be included in the final report.

Completion of the attached survey will greatly assist our efforts to meet the goals of the DCT program. An early response would be greatly appreciated.

Very truly yours,

Larry J. Graham

Larry J. Graham
Project Engineer

DIGITAL CARD TESTER (DCT)

MAINTENANCE APPLICATION CONCEPTS SURVEY

July 1977

Prepared by

A. L. Simmons

ARINC Research Corporation
a Subsidiary of Aeronautical Radio, Inc.
2551 Riva Road
Annapolis, Maryland 21401

CONTENTS

INTRODUCTION

The purpose of this survey is to obtain and catalog Digital Card Tester (DCT) application concepts related to the role(s) of a DCT within the U.S. Army. The survey also seeks data on material requirements, training, and employment limitations to provide ECOM with a more comprehensive understanding of the scope and need for a DCT in support of electronic systems using digital technology.

The survey is divided into three parts. Part I, General Information, should be completed by all. Part II should be completed by those organizations currently employing DCTs, and Part III should be completed by organizations that expect to employ a DCT within the next five years. You may respond to all three parts of the survey. Please complete all applicable parts.

If you do not have or do not anticipate having a DCT, but have knowledge of this subject, please complete applicable sections.

If the survey sheet appears to be incomplete, please feel free to supplement existing elements and to provide supporting documentation. Further, if the space provided for your answers is inadequate, please attach additional sheets. The completed survey sheet and all supporting documentation provided will be forwarded to ECOM at the close of the contract. Therefore, please type or neatly print your responses.

Information related to the ECOM contract with ARINC Research Corporation, i.e., contract description, objectives, tasks, and potential benefits, are provided below.

1. Contract Description

   - Contract Title: Determine the Best Set of Characteristics for a Digital Card Tester
   - Customer: U.S. Army Electronics Command
Directorate of Maintenance
TMDE Division (DRSEL-MA-DM)
Ft. Monmouth, New Jersey
   - Contract Number: DAEA 18-72-A-0005, Delivery Order 0007, Modification 08
   - Period of Performance: May 12, 1977 - November 8, 1977
   - COR: Mr. Robert Both (AUTOVON 992-2715)

2. Contract Objectives

   - Determine the best set of characteristics for a semi-automatic general purpose digital card tester (DCT).

- Estimate the basic hardware and software costs of DCTs.
- Determine the best maintenance support applications for an Army-adopted DCT.

3. DCT Program Tasks

- Task 1 - Evaluate the DCT Market
- Task 2 - Develop and Distribute a DCT Capabilities Survey Sheet
- Task 3 - Develop and Distribute a DCT Applications Survey Sheet
- Task 4 - Review and Summarize DCT Characteristics
- Task 5 - Develop a DCT Applications Concept
- Task 6 - Prepare Final Report
- Task 7 - Prepare Parameters for DCT

4. The following potential benefits are anticipated as a result of the DCT Program:

- A list of DCTs that are currently available OTS will be prepared.
- The respective capabilities and constraints of each DCT surveyed will be identified, cataloged, and displayed for comparative analysis.
- DCT capabilities vs cost data for a tradeoff analysis between general purpose TMDE, DCT, and ATE will be available.
- Cost data related to the development of Test Program Sets (TPS) for DCTs will be available to assist in determining the "break-even point" between DCTs and ATE.
- Current and envisioned DCT maintenance concepts will be cataloged for subsequent review and analysis.
- Finally, it will be possible to procure a standard supportable general purpose OTS DCT that will reduce overall logistics cost, enhance mission performance, and eliminate unnecessary proliferation in the ATE field.

If you have questions concerning the program, please contact the COR, Mr. Robert Both. If you have questions related to the survey, please call either of the following representatives of ARINC Research Corporation, Annapolis, Maryland:

Mr. Albert L. Simmons - (301) 224-4000, ext. 369

Mr. Larry J. Graham - (301) 224-4000, ext. 400

The completed survey must be received by ARINC Research Corporation not later than August 19, 1977, to ensure that it will be included in the final report. Your cooperation and timely response will be appreciated.

DIGITAL CARD TESTER (DCT) CONSTRAINTS

The following "constraints" were part of the criteria by which DCT equipment was selected for this survey. These constraints were presented to interested parties at Fort Monmouth on June 7, 1977:

- The DCT must be procurable off-the-shelf (OTS).
- The DCT must be portable and capable of operating from either 50/60 or 400 Hz 115/230 Vac power sources. (The DCT can be modified to meet this constraint.)
- The DCT must not exceed three separate units, exclusive of program files, accessories, and external test equipment.
- The total weight of the DCT must not exceed 200 pounds (90.72 kilograms), with no individual unit exceeding 95 pounds (43.1 kilograms).
- The cost of each DCT system (less TPS cost) must not exceed $50,000.
- The DCT must be programmable, in the field, by a skilled electronics repair technician.

MAKES AND MODELS OF DIGITAL CARD TESTERS

The following is a representative sample of DCTs that will be included in the survey (the list should not be considered complete):

Manufacturer	Model Number/Name
Bendix	13A9070 (Herbie)
Data Tester	Series 5800
Digital General	Elf
Fluke	3010A
General Dynamics	ICT-105
Hughes	HC-192
Micro System	Series 500
Technology Marketing	Series 5000
Testline	2200

PART I

1.0 General Information: It is assumed that your organization is currently employing a DCT or anticipating use of a DCT sometime in the future.

1.1 Points-of-Contact: Please list those persons that can be contacted by either ECOM or ARINC Research Corporation should any questions arise concerning this survey.

Name	Office Symbol	AUTOVON	Commercial Phone
______	______	______	______
______	______	______	______

1.2 Please provide comments on the "constraints" shown on page 3:

______

______

______

1.3 Are there any makes/models of DCT (other than those listed on page 3)) that you would recommend as a potential U.S. Army standard DCT? Yes__ No__ If yes, please list the manufacturer's name(s) and model number(s):

Manufacturer's Name	Model Number
______	______
______	______
______	______

1.4 Do you believe a DCT is essential to the availability or maintainability of any current or planned electronic systems utilizing digital technology?

Yes___No___ Please qualify your answer: ______

______

______

______

1.5 Do you believe that (or has it been demonstrated that) a DCT can reduce the number of different types of general/special purpose TMDE required to support your current/planned electronic system?

Yes___No___ Please qualify your answer: ______

______

______

______

1.5.1 Will a DCT reduce the overall quantity of TMDE required, e.g., from 3 oscilloscopes to 2 oscilloscopes, if not the number of different types of TMDE?

Yes___No___ Please qualify your answer:____________________

1.5.2 Can you provide supporting data for either of the above responses to ECOM?

Yes___No___ Please describe the type of data available:____________________

2.0 Limitations

2.1 Assuming the U.S. Army had a standard DCT, indicate the physical characteristics or limiting factors that would have an impact on your organization/project/program.

2.1.1 The dimensions should not exceed:

Width____________ Height____________ Depth____________

2.1.2 The weight should not exceed:____________________

2.1.3 The desired MTBF:____________________

2.1.4 The desired MTTR:____________________

2.1.5 Describe environmental limitations:____________________

2.1.6 Others:____________________

2.2 Will the PCBs in your environment be conformally coated? Yes___ No___
If yes, does your maintenance scheme include any methodology or equipment for removing and replacing the conformal coating?

Please describe:____

____

____

____

2.3 Do you have or do you anticipate having a requirement for a DCT to fault-isolate to a PCB or group of PCBs within a system or LRU? Yes___ No___

If yes, please describe your requirements:______________________

____

____

____

2.4 Describe (in general terms) the type of logic technology, circuitry, or chips used (or anticipated) in the make-up of the PCBs, e.g., TTL, CMOS, I^2L, DDC, Bubble, etc., that are supported (or could be supported) by a DCT.

____

____

____

2.4.1 Indicate the maximum Clock Rate:___________________________

2.4.2 Indicate the following:

Access time__________ Cycle time__________ Gate switching time__________

2.4.3 Indicate the maximum number of bits at each of those rates (buffer-size requirement):

Access time__________ Cycle time__________ Gate switching time__________

3.0 Test Program Set (TPS) Development

3.1 A TPS can be developed from many different sources. Given a choice, indicate the "best" and worst" sources from those identified below, based on your experience:

Prime system manufacturer__________________________________

DCT manufacturer____

U.S. Army Depot____

By contract to a software house____________________________

U.S. Army technicians in the field ______

Other(s) ______

Please qualify your answers: ______

______

______

______

3.2 Assuming a TPS has been fielded, who should maintain the configuration control of the TPS? Indicate the "best" and worst" sources from those identified below:

Commodity Manager ______

Prime system manufacturer ______

DCT manufacturer ______

U.S. Army Depot ______

U.S. Army technicians in the field ______

Other(s) ______

Please qualify your answers: ______

______

______

______

3.2.1 Assuming control over a TPS has been established, who should do the actual updating and/or modifying of the TPS? Indicate "best" and "worst" sources from those identified below:

Prime system manufacturer ______

DCT manufacturer ______

U.S. Army Depot ______

Contract to commercial software house ______

U.S. Army technicians in the field ______

Other(s) ______

Please qualify your answers: ______

______

______

______

3.3 Describe the system you currently have or envision for management of TPSs within your organization: ______________________________

____

____

____

3.4 What level of fault detection/isolation is currently available or is envisioned as being required for a DCT? Check (√) the appropriate space:

Go/No-Go only ______________________________

Go/No-Go and circuit (pin) isolation combined ______________________________

Go/No-Go, circuit (pin), and component isolation combined ______________________________

Please qualify your answer: ______________________________

____

____

____

3.4.1 Indicate with a checkmark (√) the desired fault-detection/isolation level(s) by (PCB) type/complexity:

	Level of Complexity		
PCB Type	Go/No-Go	Circuit (Pin) Isolation	Component Isolation
Analog	______	______	______
Hybrid	______	______	______
Digital	______	______	______
SSI	______	______	______
MSI	______	______	______
LSI	______	______	______

3.5 Test resolution can be expressed as a percentage of confidence that a TPS will fault-detect/isolate to the desired programmed level. What confidence level do you require in TPS? Put a checkmark (√) in the appropriate space:

Over 99 percent ______________________________

95 to 99 percent ______________________________

90 to 95 percent ______________________________

85 to 90 percent ______________________________

Please qualify your answer:______________________________________

3.6 Please indicate with a checkmark (✓) the test method(s) most suited to the support of your equipment

Edge connector______________________________________

Guided probe______________________________________

Edge connector with guided probe____________________________

"Smart" probe______________________________________

Other(s)____

Please qualify your answer:______________________________________

4.0 Training

4.1 Assuming the U.S. Army had a standard DCT, complete the following questions.

4.2 Should the DCT training program be a part of the End Item (E/I) training course?

Yes___ No___ Please qualify your answer:____________________________

4.2.1 Should the training course include [please check (✓) the appropriate space]:

DCT operating training?________________________________

DCT programming training?______________________________

DCT repair training?__________________________________

4.3 If your organization is now utilizing a DCT, please describe the training program(s) and indicate whether they include all of the above types of training:____________________________________

PART II

5.0 Material on Hand: If your organization currently utilizes a DCT, please complete the following:

5.1 Identify each DCT by manufacturer's name, model number, and quantity on hand, and indicate with a checkmark (✓) whether the DCT is special purpose (can be used to support only one end item) or general purpose:

Manufacturer's Name	Model Number	Quantity on Hand	Special Purpose	General Purpose

5.2 Identify the End Items (E/I) supported by DCT model number:

E/I Manufacturer	E/I Model Number	DCT Model Number

5.3 For each E/I listed in Paragraph 5.2, determine the number and types of Printed Circuit Boards (PCB) that have a validated Test Program Set (TPS). Please record the number of PCBs correlated with the E/I model number:

	Numbers of PCBs with Validated TPS			
E/I Model Number	Analog	Hybrid	Digital	Total
Total				

5.3.1 Indicate and/or estimate the number of PCBs that do not have a TPS for the E/Is listed above:

E/I Model Number	Analog	Hybrid	Digital	Total

5.3.2 Do you plan to obtain TPS for some or all of the PCBs listed in Paragraph 5.3.1?

Yes___No___ Please qualify your answer:______________________________

____

____

____

5.3.3 Have you budgeted funds for this purpose? Yes___No___ Indicate funding by fiscal year:

FY78_________ FY79_________ FY80_________ FY81_________ FY82_________

5.4 List and describe the component elements that make up a TPS (Note: if the TPS elements vary between DCTs, describe and list each separately, identifying the DCT concerned):______________________________

____

____

____

5.4.1 Identify and describe the source(s) of the TPS for each DCT listed in Paragraph 5.1:

Source of TPS	DCT Model Number
____________________	____________________
____________________	____________________
____________________	____________________

5.4.2 *What was the average cost per TPS for each of the DCTs identified in* Paragraph 5.1 above?

DCT Model Number	TPS Average Cost
____________________	____________________
____________________	____________________
____________________	____________________
____________________	____________________

6.0 Maintenance Concept - Current

6.1 For each DCT model listed in Paragraph 5.1 above, describe in detail its current role(s) in the maintenance support concept for each E/I supported:

____

____

____

6.1.1 Indicate with a checkmark (√) the level(s) of maintenance at which the DCT is employed:

	Level of Maintenance						
DCT Model Number	O	DS	GS	D	On-Site	Off-Site	Others*
______	___	___	___	___	___	___	___
______	___	___	___	___	___	___	___
______	___	___	___	___	___	___	___

*Describe: ______________________________

____

____

____

7.0 DCT Description

7.1 Indicate the dimensions, weight, MTBF, and MTTR for each of the DCTs listed in Paragraph 5.1 above (estimate data if unknown):

DCT Model Number	Width	Height	Depth	Weight	MTBF	MTTR
______	___	___	___	___	___	___
______	___	___	___	___	___	___
______	___	___	___	___	___	___

7.1.1 What MTBF and MTTR would be acceptable? MTBF______ MTTR______

7.1.2 Describe any environmental limitations by DCT model number:

____

____

____

7.1.3 Describe any environmental requirements by DCT maintenance applications concept: ______________________________

____

____

____

PART III

8.0 Material Requirements (For Part III it is assumed that your organization anticipates employing a DCT within the next five years.)

8.1 Estimate the quantity of DCTs required for each End Item (E/I) or program name to be supported (in part or whole) by a DCT:

Fiscal Year by Quarters

E/I Model NR/	78				79				80				81				82			
Program Name	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4

8.2 Estimate by E/I Number/Program Name the quantity of Printed Circuit Cards (PCB) by type that you anticipate will require a TPS:

E/I Model NR/	Type of PCB			
Program Name	Analog	Hybrid	Digital	Total

8.3 What is the average amount you have budgeted/planned to budget per TPS?

$______________ Comment: ____

____

____

____

9.0 Maintenance Concept - Envisioned/Planned

9.1 Describe the envisioned/planned role(s) for the DCT in the maintenance support concept for each E/I and/or program name: ______________________

____

____

____

9.2 Indicate with a checkmark (✓) the level(s) of maintenance at which the DCT will be employed:

E/I Model NR/ Program Name	O	DS	GS	D	On-Site	Off-Site	Other*

*Describe: ____________________

9.3 Are you currently considering any model(s) of DCT? Yes__ No__
Please list:

Manufacturer's Name	Model Number	Associated E/I or Program

9.4 What components do you anticipate will make up a TPS? Please describe:

____

This completes the Survey Sheet. Thank you for your cooperation. Please return to:

ARINC Research Corporation
2551 Riva Road
Annapolis, Maryland 21401
ATTN: DC^3/TSP (L. Graham)

APPENDIX E

LIST OF U. S. ARMY SURVEY PARTICIPANTS

1. PM, REMBASS, Fort Monmouth, N.J. 07703
   Mr. Blue, DRCPM-RBS-L

2. PM, ATACS, Fort Monmouth, N.J. 07703
   Mr. Prince, DRCPM-ATC-TM

3. PM, Firefinder, Fort Monmouth, N.J. 07703
   Mr. Maryanski, DRCPM-FF-LM

4. DIR, R&D TECH SUP ACT, Fort Monmouth, N.J. 07703
   Mr. Wheeler, DRSEL-GG-C

5. PM, ARTADS, Fort Monmouth, N.J. 07703
   Mr. Kasian, DRCPM-TDS-LO-E

6. PM, NAVCON, Fort Monmouth, N.J. 07703
   Mr. Lucas, DRCPM-NC-TM

7. CDR, US Army Electronics Command, Fort Monmouth, N.J. 07703
   Mr. George Simmons, DRSEL-MA-SA

8. CDR. US Army Electronics Command, Fort Monmouth, N.J. 07703
   Mr. Henry Przybylowski, DRSEL-MA-SC

9. CDR, US Army Test and Evaluation Command,
   Aberdeen Proving Ground, MD. 21005
   Mr. Metroka, DRSTE-RM,

10. CDR, Sacramento Army Depot, Sacramento, CA. 95813
    DRXSA-MPE-3

11. CDR, US Army Materiel Systems Analysis Activity,
    Aberdeen Proving Ground, MD. 21005
    Mr. Dan Lynch, Attn: DRXSY-CC

12. CDR, US Army Electronics Command, Fort Monmouth, N.J. 07703
    DRSEL-MA-C

13. CDR, US Army Electronics Command, Fort Monmouth, N.J. 07703
Mr. Joe Gross, DRSEL-MA-CA

14. CDR, US Army Electronics Command, Fort Monmouth, N.J. 07703
Mr. Al Miller, DRSEL-MA-CA, (201) 522-2519

15. CDR, US Army Electronics Command, Fort Monmouth, N.J. 07703
Mr. Bob Moeller, DRSEL-MA-CA

16. CDR, US Army Electronics Command, Fort Monmouth, N.J. 07703
Mr. Sartore, DRSEL-TL-IR, System: SEM Modules

17. PM, ATSS, Fort Monmouth, N.J. 07703
Mr. Nick Karalekas

18. HQ. US Army Armament Materiel Readiness Command, Rock Island, IL 61201
Mr. Bard, DRSAR-MAT

19. CDR, US Army Armament Research & Development Command,
Dover, N.J. 07981
Attn: DRDAR-PM, Col. Henry

20. CDR, US Army Tank-Automotive Materiel Readiness Command,
Warren, Michigan 48090
Mr. Martin, DRSTA-MST

21. CDR, US Army Tank-Automotive Materiel Readiness Command,
Warren, Michigan 48090
Maj. A. Woytek, DRSTA-MST

22. CDR, US Army Tank-Automotive Materiel Readiness Command,
Warren, Michigan 48090
Mr. D. Sarna, DRDTA-RGD,

23. CDR, US Army Tank-Automotive Materiel Readiness Command,
Warren, Michigan 48090
Mr. J. Phillips, DRDTA-RGD

24. CDR, USA Satellite Communications Command,
Fort Monmouth, N.J. 07703
Mr. Ryan, DRCPM-SC-8B

25. CDR, US Army Maintenance Management Center, Lexington, KY. 40511
Mr. Winglewich, DRXCT-TR

26. CDR, Harry Diamond Laboratories,
Powder Mill Road, Adelphi, MD. 20783
Attn: DRXDO-EDG

27. DIR, US Army Materiels & Mechanics Research Center
Watertown, MA. 02172
Attn: DRXMR-AE

28. CDR, US Army Mobility Equipment Research & Development Command,
Fort Belvoir, VA. 22060
Attn: DRDME-HM

29. CDR, US Army NATICK Research & Development Command,
NATICK, MA. 01760
Attn: DRXNM-EPE

30. CDR, Anniston Army Depot, Anniston, AL. 36201
Attn: DRXAN-DQ-QC

31. CDR, Corpus Christi Army Depot, Corpus Christi, Texas 78419
Attn: DRXAD-EMHR

32. CDR, Letterkenny Army Depot, Chambersburg, PA. 17201
Attn: DRCLE-QC

33. CDR, New Cumberland Army Depot, New Cumberland, PA. 17070
Attn: DRXNC-SM-M

34. CDR, Pueblo Army Depot, Pueblo, CO. 81001
Attn: DRXPJ-ME

35. PM, Sincgars, Fort Monmouth, N.J. 07703
Mr. Norm Gionet, DRCPM-GARS-LM

36. DIR, ET2D LAB, Fort Monmouth, N.J. 07703
Mr. Sacane, DRSEL-TL-MI

37. CDR, US Army Communications Command, Fort Huachuca, AZ. 85613
CW4 Charles Hendricks, CC-LOG-SM-M4

38. CDR, US Army Electronics Materiel Readiness Activity,
Vint Hill Farms Station, Warrenton, VA. 22186
Mr. Shelton, DRXEM-NM-S

39. CDR, US Army Electronics Materiel Readiness Activity,
Vint Hill Farms Station, Warrenton, VA. 22186
CW2 Larry Bourn, DRXEM-ES-A

40. CDR, US Army Electronics Materiel Readiness Activity,
Vint Hill Farms Station, Warrenton, VA. 22186
Mr. Harry Michelitch, DRXEM-NM-S

41. CDR, Tobyhanna Army Depot, Tobyhanna, PA. 18466
Mr. John Frace, DRXTO-MI-P

42. CDR, USAECOM, COM/ADP LAB, Fort Monmouth, N.J. 07703
Mr. Taper, DRSEL-RF-I

43. CDR, USA Communications Systems Agency, Fort Monmouth, N.J. 07703
Mr. Thomas Terrana, USACSA-CCM-EQ

44. CDR, US Army Aviations Systems Command, P.O. Box 209
St. Louis, MO. 63166
Attn: DRSAV-FEM

45. CDR, US Army Missile Materiel Readiness Command,
Redstone Arsenal, AL. 35809
Attn: DRSMI-NLC

46. CDR, US Army Tank-Automotive Research & Development Command
Warren, MI. 48090

47. CDR, US Army Troop-Support Command, 4300 Goodfellow Blvd.
St. Louis, MO. 63120
Attn: DRSTS-MLL

48. CDR, Frankford Arsenal, Phil, PA. 19137
Attn: SARFA-FCF

49. CDR, Red River Army Depot, Texarkana, Texas 75501
Attn: DRXRR-TE

50. CDR, Sharpe Army Depot, Lathrop, CA. 95330
Attn: DRXSH-SO

51. CDR, Toole Army Depot, Tooele, VT. 84074
Attn: DRXTE-SEQ

52. CDR, US Army Electronics Command, COM/ADP LAB, Fort Monmouth, N.J. 07703
Mr. Shirley, DRSEL-NL-D-4

53. CDR, US Army Electronics Command, EW LAB, Fort Monmouth, N.J. 07703
Mr. Weiner, DRSEL-WL-C, 535-3151

54. PM, MSCS, Fort Monmouth, N.J. 07703
Mr. Taylor, DRCPM-MSCS-LM

55. PM, MSCS, Fort Monmouth, N.J. 07703
Mr. Drummond, DRCPM-MSCS-LM, 535-3193

56. PM, Special Electronic Mission Aircraft (SEMA) Materiel Readiness
US Army Aviation Systems Command, St. Louis, MO. 63166
Attn: DRCPM-AE

57. PM, Army Tactical Data Systems, US Army Electronics Command,
Fort Monmouth, N.J. 07703
Attn: DRCPM-TDS-LO-E, Mr. Kasian

58. PM, Multi-Service Communications System, US Army Electronics Command,
Fort Monmouth, N.J. 07703
Attn: DRCPM-MSCS-LM

59. PM, Signal Intelligence/Electronics Warfare (SIGINT/EW) Materiel Readiness, US Army Electronics Command, Fort Monmouth, N.J. 07703
Mr. Gimpel, Attn: DRCPM-SIEW-TM

60. PM, FAMACE, Fort Belvoir, VA. 22060
Attn: DRCPM-FM

61. PM, CHAPARRAL/FARR, US Army Missile Command, Redstone Arsenal, AL. 35809
Attn: DRCPM-CF

62. PM, DRAGON, US Army Missile Command, Redstone Arsenal AL. 35809
Attn: DRCPM-MWE

63. PM, General Support Rocket System, US Army Missile Command, Redstone Arsenal, AL. 35809
Attn: DRCPM-RS

64. PM, HAWK, US Army Missile Command, Redstone Arsenal AL. 35809
Attn: DRCPM-HAEE

65. PM, Hellfire Missile System, US Army Missile Command Redstone Arsenal, AL. 35809
Attn: DRCPM-HFS

66. PM, High Energy Laser System, US Army Missile Command, Redstone Arsenal, AL. 35809
Attn: DRCPM-HEL

67. PM, Lance, US Army Missile Command, Redstone Arsenal, AL. 35809
Attn: DRCPM-LC-EE

68. PM, Pershing, US Army Missile Command, Redstone Arsenal, AL. 35809
Attn: DRCPM-PE-EG

69. PM, Precision Laser Designators, US Army Missile Command, Redstone Arsenal, AL. 35809
Attn: DRCPH-LDS

70. PM, 2.75 Rocket System, US Army Missile Command, Redstone Arsenal, AL. 35809
Attn: DRCPM-RK

71. PM, Stinger, US Army Missile Command, Redstone Arsenal, AL. 35809
Attn: DRCPM-MPS

72. PM, TOW, US Army Missile Command, Redstone Arsenal, AL. 35809
Attn: DRCPM-TO

73. PM, US Roland, US Army Missile Command, Redstone Arsenal, AL. 35809
Attn: DRCPM-ROL-S

74. PM, VIPER, US Army Missile Command, Redstone Arsenal, AL. 35809
Attn: DRCPM-VI

75. PM, 1 1/4 Ton Commercial Truck Systems, US Army Tank-Automotive Materiel Readiness Command, MAMP, Bldg., 2, Warren, MI. 48090
Attn: DRCPM-CTT

76. PM, Heavy Equipment Transporter, US Army Tank-Automotive Materiel Readiness Command, Warren, MI. 48090
Attn: DRCPM-HT

77. PM, M113A1 Family of Vehicle Readiness, US Army Tank-Automotive Materiel Readiness Command, MAMP, Bldg. 2, Warren, MI. 48090
Attn: DRCPM-M113

78. PM, M60 Tank Development, Universal City Professional Building 28150 Dequindre, Warren, MI. 48092
Attn: DRCPM-M60TD-L

79. PM, M60 Tank Production, Universal City Professional Building, 28150 Dequindre, Warren, MI. 48092
Attn: DRCPM-M60TP-L

80. PM, Improved Tow Vehicle (ITV), US Army Tank-Automotive Research and Development Command, Warren, MI. 48090
Attn: DRCPM-FV

81. PM, Amphibians and Watercraft, US Army Troop Support Command, 4300 Goodfellow Blvd., St. Louis, MO. 63120
Attn: DRCPM-AWC

82. PM, Advanced Attack Helicopter, US Army Aviation Systems Command, St. Louis, MO 53165
Attn: DRCPM-AAH-TM-A

83. PM, DCS (Army) Communications Systems, Fort Monmouth, N.J. 07703
Attn: DRCPM-EQ

84. PM, Fighting Vehicle Systems, Universal City Professional Building 28150 Dequindre, Warren, MI. 48092
Attn: DRCPM-FVS

85. PM, Mobile Electric Power, 7500 Backlick Road, Springfield, VA. 22150
Attn: DRCPM-MEP-TM

86. PM, Nuclear Munitions, Dover, N.J. 07801
Attn: DRCPM-NUC

87. PM, Patriot Missile System, US Army Materiel Development & Readiness Command, Redstone Arsenal, AL. 35809
Attn: DRCPM-MD-TG

88. PM, Training Devices, Naval Training Equipment Center, Orlando, FL. 32813
Attn: DRCPM-TND-LM

89. PM, Utility Tactical Transport Aircraft System, US Army Aviation System Command, St. Louis, MO. 63166

90. PM, XM-1 Tank System, Universal City Professional Building, 28150 Dequindre, Warren, MI. 48092
Attn: DRCPM-GCM-L

APPENDIX F

LIST OF DCT MANUFACTURERS

1. The Bendix Corporation
   Navigation and Control Group
   Teterboro, New Jersey 07608

2. Data Test Corporation
   2450 Whitman Road
   Concord, California 94518

3. Digital General Corporation
   University Circle Research Center
   11000 Cedar Avenue
   Cleveland, Ohio 44106

4. Fluke-Trendar
   500 Clyde Avenue
   Mountain View, California 94043

5. General Dynamics
   Electronics Division
   P. O. Box 81127
   San Diego, California 92138

6. Hughes Aircraft Company
   Ground Systems Group
   Fullerton, California 92634

7. GenRad
   Test Systems Division
   300 Baker Avenue
   Concord, Massachusetts 01742

8. Mirco Systems Division
   10888 North 19th Avenue
   Phoenix, Arizona 85029

9. Technology Marketing Incorporated
   3170 Red Hill Avenue
   Costa Mesa, California 92626

10. Testline
    N. Brevard Industrial Park
    P. O. Box 5686
    Titusville, Florida 32780

11. Systron-Donner Corporation
    Data Products Division
    935 Detroit Avenue
    Concord, California 94518

APPENDIX G

TPS COST, CONFIDENCE, AND RUN-TIME DATA

Each DCT manufacturer was asked to estimate the "run time" of four hypothetical PCBs on the instrument addressed by his survey form -- i.e., the time (in seconds) that it would take the DCT to fault-detect/isolate to a predetermined test level. Table G-1 depicts the results. Table G-2 summarizes the run-time ranges. ARINC Research Corporation experience indicates that it is reasonable to conclude that a DCT can fault-detect/ isolate much more rapidly than a complement of general purpose TMDE and "hot" mock-ups.

In Section 7 of the survey form, questions were asked regarding the development of TPS; these questions were centered on the PCBs described in the five appendixes to the DCT Capability Survey form (Appendix C). Each of the appendixes provided documentation related to a PCB currently in the U.S. Army inventory, including, as a minimum, a schematic, a discussion on the theory of operation, an illustrated parts breakdown, and a parts list. The purpose of the survey questions was to determine if the documentation provided was adequate for developing a TPS, the cost of TPS development, and an expected level of test confidence for a TPS. The documentation provided was adequate for all of the DCT manufacturers surveyed to estimate cost and confidence levels for the five PCBs. The estimated cost and expected levels of confidence in test results are shown in Tables G-3 through G-7, with each table referring to a specific PCB, i.e., an appendix of the DCT Capabilities Survey form.

In Table G-8 the TPS cost, confidence level, and test times are summarized in a series of low to high ranges for the five PCBs.

Table G-9 illustrates the estimated average cost for the five PCBs to the maximum level of fault detection/isolation, as well as for a go/no-go test for each of the DCTs surveyed.

Table G-1. ESTIMATED DCT RUN TIMES IN SECONDS (Source: Para. 4.3, Capabilities Survey)

Manufacturer	Model Number	Hybrid, 10 MSI ICs			Digital, 50 SSI ICs			Digital, 25 MSI ICs			Digital, 5 LSI ICs		
		Go/No-Go	Circuit (Pin)	Component	Go/No-Go	Circuit (Pin)	Component	Go/No-Go	Circuit (Pin)	Component	Go/No-Go	Circuit (Pin)	Component
Bendix	13A9070	2	3	4	1.5	2	3	3	4	6	15	16	17
Data Tester	5800	300	300	1200	15	15	180	15	15	120	60	60	60
Digital General	ELF	3	3	300	3	3	600	3	3	600	20	20	900
Fluke	1000A				2	60	300	2	60	480	2	60	720
	3010A				2	60	240	2	60	420	2	60	600
General Dynamics	ICT-105	60*	300	600	1	10	300	2	20	160	4	40	180
Hughes	HC-192	1	60	240	2	60	420	2	60	420	10	60	240
Mirco Systems	520	1	1	**	1	1	**	1	1	**	1	1	**
Testline	2200	60	60	60	240	240	240	120	120	120	60	60	60
	2300	60	60	60	240	240	240	120	120	120	60	60	60

Level of Fault Detection/Isolation by PCB Type

*See survey form for hybrid PCB.

**Run time for components depends on operator skill.

Table G-2. ESTIMATED DCT RUN TIME RANGES IN SECONDS

Level of Fault Detection/Isolation	Run Time (Minutes) by PCB Type				
	Hybrid, 10 MSI ICs	Digital, 50 SSI ICs	Digital, 25 MSI ICs	Digital, 5 LSI ICs	Low-High, All PCBs
Go/No-Go	1 to 300	1 to 240	1 to 120	1 to 60	1 to 300
Circuit (Pin)	1 to 300	1 to 240	1 to 120	1 to 60	1 to 300
Component	60 to 1200	3 to 600	6 to 600	17 to 900	3 to 1200

Note: Data supplied by respective manufacturers.

Table G-3. DISTORTION GATE GENERATOR 1A2A6 (Source: Appendix A, Capabilities Survey)

Manufacturer	Model Number	TPS Cost for Maximum Level of Fault Detection/Isolation: Documentation	Interface Device	Programming	Total	Cost of TPS Copies	Level of Confidence (Percent)	Test Time* (Seconds)	TPS Cost for Go/No-Go Indication Only: Documentation	Interface Device	Programming	Total	Level of Confidence (Percent)	Test Time* (Seconds)
Bendix	13A9070	$100	$500	$5000	$5600	$100	96	1	$ 50	$500	$2500	$3050	98	0.5
Data Tester	5800	75	200	1400	1675	50	99	15	75	200	1400	1675	99	75
Digital General	ELF	100	0	475	575	50	99	2	50	0	475	525	99	2
Fluke	1000A 3010A	750 750	450 450	300 250	1500 1450	500 500	99 99	5 4	750 750	450 450	300 250	1500 1450	99 99	5 4
General Dynamics	ICT-105	750	350	800	1300	100	95	240	125	350	667	1142	95	2
Hughes	HC-192	150	400	500	1050	150	98	2	50	400	400	850	98	2
Mirco Systems	520	100	300	1000	1400	300	95	1	50	300	900	1250	90	1
Testline	2200 2300	60 60	0 0	100 100	160 160	100 100	96 96	120 120	60 60	0 0	100 100	160 160	96 96	120 120

*Estimated "run time".

Table G-4. ISLS PULSE TIMER SINGE-SHOT (Source: Appendix B, Capabilities Survey)

Manufacturer	Model Number	TPS Cost for Maximum Level of Fault Detection Isolation: Documentation	Interface Device	Programming	Total	Cost of TPS Copies	Level of Confidence (Percent)	Test Time* (Seconds)	TPS Cost for Go/No-Go Indication Only: Documentation	Interface Device	Programming	Total	Level of Confidence (Percent)	Test Time* (Seconds)
Bendix	13A9070	$100	$700	$4000	$4800	$100	92	1	$ 50	$700	$1800	$2550	92	0.5
Data Tester	5800	75	180	1120	1480	50	99	15	75	180	1120	1480	99	15
Digital General	ELF	100	0	350	450	50	99	2	50	0	350	400	99	2
Fluke**	1000A 3010A	750 750	500 500	350 300	1600 1550	525 525	99 99	20 10	750 750	500 500	350 300	1600 1550	99 99	20 10
General Dynamics**	ICT-105	113	350	[illegible]	1063	100	95	240	103	350	545	998	99	2
Hughes†	HC-192	225	400	800	1425	225	95	240	125	400	700	1225	95	2
Mirco Systems	520	100	300	800	1200	300	95	1	50	300	700	1050	75	1
Testline	2200 2300	45 45		75 75	120 120	100 100	96 96	90 90	45 45		75 75	120 120	96 96	90 90

*Estimated "run time".
**May require oscilloscope.
†Required oscilloscope.

Note: Data supplied by respective manufacturers.

Table G-5. MODULAR CARRIER GENERATOR CIRCUIT CARD ASSEMBLY 10281636 (Source: Appendix C, Capabilities Survey)

Manufacturer	Model Number	TPS Cost for Maximum Level of Fault Detection Isolation				Cost of TPS Copies	Level of Confidence (Percent)	Test Time* (Seconds)	TPS Cost for Go No-Go Indication Only				Level of Confidence (Percent)	Test Time* (Seconds)
		Documentation	Interface Device	Programming	Total				Documentation	Interface Device	Programming	Total		
Bendix	13A9070	$ 100	$500	$5000	$5600	$100	92	2	$ 50	$500	$4000	$4550	92	2
Data Tester	5800	75	250	1500	1825	50	98	15	75	250	1500	1825	98	15
Digital General	ELF	100	0	500	600	50	98	5	50	0	500	550	98	5
Fluke	1000A 3010A	1000 750	450 450	350 300	1850 1500	500 500	99 99	5 4	1000 750	450 450	350 300	1850 1500	99 99	5
General Dynamics	ICT-105	225	350	1200	1775	100	90	300	173	350	923	1446	90	
Hughes**	HC-192	180	400	1000	1580	180	95	4	100	400	850	1350	95	[illegible]
Mirco Systems	520	100	300	1400	1800	300	95	1	50	300	1200	1550	95	1
Testline	2200 2300	96 96	0 0	160 160	256 250	100 100	96 96	180 180	96 96	0 0	160 160	256 256	96 96	[illegible] 180

*Estimated "run time".
** Requires oscilloscope.

Table G-6. RF SWITCH DRIVER CARD A32A2 (Source: Appendix D, Capabilities Survey)

Manufacturer	Model Number	TPS Cost for Maximum Level of Fault Detection/ Isolation				Cost of TPS Copies	Level of Confidence (Percent)	Test Time* (Seconds)	TPS Cost for Go/No-Go Indication Only				Level of Confidence (Percent)	Test Time* (Seconds)
		Documentation	Interface Device	Programming	Total				Documentation	Interface Device	Programming	Total		
Bendix	13A9070	$ 100	$700	$5000	$5800	$100	80	1	$ 50	$700	$1200	$1950	95	0.2
Data Tester	5800	75	360	1500	1935	50	95	15	75	360	1500	1935	95	15
Digital General	ELF	100	300	200	600	350	95	15	50	300	200	550	95	15
Fluke**	1000A 3010A	750 1000	550 550	300 300	1550 1850	600 600	99 99	20 10	[illegible] 1000	550 550	300 300	1550 1850	99 99	20 10
General Dynamics	ICT-105	83	350	600	1033	100	90	360	75	350	545	970	90	30
Hughes†	HC-192	225	400	600	1225	225	75	250	125	400	500	1025	60	1
Mirco Systems	520	100	300	500	900	300	95	1	50	300	450	800	95	1
Testline	2200 2300													

*Estimated "run time".
**May require oscilloscope.
†Requires ancillary power supply.

Note: Data supplied by respective manufacturers.

Table G-7. SIXTEEN-BIT SHIFT REGISTER CIRCUIT CARD ASSEMBLY 10281707 (Source: Appendix E, Capabilities Survey)

Manufacturer	Model Number	TPS Cost for Maximum Level of Fault Detection/ Isolation				Cost of TPS Copies	Level of Confidence (Percent)	Test Time* (Seconds)	TPS Cost for Go/No-Go Indication Only				Level of Confidence (Percent)	Test Time* (Seconds)
		Documentation	Interface Device	Programming	Total				Documentation	Interface Device	Programming	Total		
Bendix	13A9070	$100	$700	$4000	$4800	100	99	5	$ 50	$700	$2500	$3250	99	0.5
Data Tester	5800	75	200	1400	1675	50	99	15	75	200	1400	1675	99	15
Digital General	ELF	100	100	300	600	150	99	5	50	100	300	450	99	5
Fluke	1000A	750	450	250	1450	500	99	5	750	450	250	1450	99	5
	3010A	750	450	250	1450	500	99	4	750	450	250	1450	99	4
General Dynamics	ICT-105	90	350	480	920	100	95	160	82	350	436	868	95	2
Hughes	HC-192	150	400	500	1050	150	98	2	50	400	400	850	98	2
Mirco Systems	520	100	300	750	1150	300	95	1	50	300	650	1000	95	1
Testline	2200	36	N/A	60	96	100	96	60	36	N/A	60	96	96	60
	2300	36	N/A	60	96	100	96	60	36	N/A	60	96	96	60

*Estimated "run time".

Note: Data supplied by respective manufacturers.

Table G-8. TPS COST, CONFIDENCE, AND TEST TIME RANGES

PCB Description	Capabilities Survey Appendix	Cost (in Dollars)								Level of Confidence (Percent)		Test Time (Seconds)	
		Documentation		Interface Device		Programming		Total					
		Low	High	Low	High	Low	High	Low	High	Low	High	Low	High
Part I - Maximum Level of Fault Detection/Isolation													
Distortion Gate Generator 1A2A6	A	60	750	0	500	100	5000	160	5600	95	99	1	240
ISLS Pulse Time Single Shot	B	45	750	0	700	75	4000	120	4800	92	99	1	240
Modular Carrier Generator Circuit Card Assembly 10281636	C	75	1000	0	500	160	5000	256	5600	90	99	1	300
RF Switch Driver Card A32A2	D	75	1000	300	700	300	5000	500	5800	75	99	1	360
Sixteen-Bit Shift Register Circuit Card Assembly 10281707	E	36	750	0	700	60	4000	96	4800	95	99	1	160
Part II - Go/No-Go Only													
Distortion Gate Generator 1A2A6	A	50	750	0	500	100	2500	160	3050	90	99	0.5	120
ISLS Pulse Time Single Shot	B	45	750	0	700	75	1800	120	2550	75	99	0.5	90
Modular Carrier Generator Circuit Card Assembly 10281636	C	50	1000	0	500	160	4000	256	4550	90	99	1	180
RF Switch Driver Card A32A2	D	50	1000	300	700	300	1200	450	1950	60	99	0.2	30
Sixteen-Bit Shift Register Circuit Card Assembly 10281707	E	36	705	0	700	60	2500	96	3250	95	99	0.5	60

Notes:

- The interface devices in both Parts I and II are the same for each separate type of PCB.
- Depending upon the characteristics of the DCT and the PCBs, one interface device may suffice for all five PCBs.

Note: Data supplied by respective manufacturers.

Table G-9. TPS ESTIMATED AVERAGE COST			
Manufacturer	Model Number	Maximum Fault Detect/Isolate	TPS Average Cost, Go/No-Go
Bendix	13A9070	$5,320	$3,070
Data Tester	5800	1,718	1,718
Digital General	ELF	565	395
Fluke	1000A	1,590	1,590
	3010A	1,560	1,590
General Dynamics	ICT-105	1,218	1,085
Hughes	HC-192	1,266	1,060
Mirco Systems	520	1,290	1,130
Testline	2200	158	158
	2300	158	158
Average Total Cost for Five PCBs		$1,474	$1,183

Note: Data supplied by respective manufacturers.

APPENDIX H

BEST SET OF CHARACTERISTICS FOR A SEMI-AUTOMATIC GENERAL PURPOSE DIGITAL CARD TESTER (DCT)

1. DIGITAL CARD TESTER PARAMETERS

1.1 Design and Construction

Design and construction of the equipment shall comply with the requirements of MIL-T-28800 as applicable to Type III, Class 5, Style E, Color R.

1.1.1 Solid-State Construction

The equipment shall be of solid-state modular construction.

1.2 Power Source

The equipment shall operate from the Type III 50, 60, and 400 Hz single-phase 115/230 V power source requirements of MIL-T-28800. Power consumption shall not exceed 400 watts.

1.3 Dimensions and Weight

Maximum dimensions of the equipment shall not exceed 53.34 cm width by 35.56 cm height by 63.5 cm depth (21 × 14 × 25 inches). Maximum weight shall not exceed 45.36 kg (100 pounds).

1.4 Reliability and Maintainability

The mean time between failures (MTBF) of the equipment shall be at least 700 hours. The mean time to repair/restore the equipment to an operational state shall not exceed 15 minutes.

1.5 Test Method

The test method of the equipment shall be an edge connector supplemented by a guided probe. An oscilloscope may be used to assist in fault isolation to the component level.

1.5.1 Number of Pins

The equipment shall have at least 90 active bi-directional pins, which can be designed as input, output, or power.

1.6 Test Rate

The equipment shall be capable of generating a test speed up to 4 MHz.

1.7 Test Patterns

The equipment shall be capable of generating at least five different digital test patterns, each of which shall have a minimum of two test rates.

1.8 Supply Voltages

The equipment shall have at least three independent regulated supply voltage outputs that may be applied to the PCB under test. Each source shall be designed to protect both the DCT and the PCB under test.

1.8.1 Supply Voltage Range

The supply voltage range (the combination of the three power sources) shall at a minimum extend from -15 Vdc to +15 Vdc. The power out shall be at least 1 ampere.

1.8.2 Programmable Supply Voltage

The supply voltage shall be capable of being programmed in at least 1-volt steps from -3 to -15 Vdc and from +3 to +15 Vdc.

1.9 Equipment Characteristics

The equipment characteristics shall include the capability to generate a program, test the program, and transfer that program to a program storage device for future testing needs.

1.10 Self-Test

1.10.1 Operational Test

The equipment shall have the capability of verifying its operational integrity and indicating this verification to the operator prior to each testing of a printed circuit board (PCB).

1.10.2 Self-Diagnostics

The equipment shall be capable of self-diagnostics to the faulty printed circuit board.

1.11 Test Program Set (TPS)

The TPS for each PCB shall include a programmed set of instructions contained on a storage device, a method for interfacing the PCB to the DCT, and all documentation required to set up and test each PCB.

1.11.1 TPS Cost

The average cost for a TPS shall not exceed $2000.

1.11.2 Test Resolution

The average test resolution (i.e., the level of confidence required to detect or isolate a fault) for the TPS shall exceed 95 percent.

1.12 Equipment Readout

The equipment shall display the results of each test performed on the PCB under test in a manner that can easily be verified by the DCT operator.

2. ADDITIONAL DCT CHARACTERISTICS FOR CONSIDERATION

2.1 Analog Test Capability

The equipment shall have the capability of testing analog circuitry for a go/no-go indication with a 90 percent average test resolution.

2.2 External Test Rate

The equipment shall have the capability of receiving and applying an externally generated test rate of up to 12 MHz to the internal test patterns.